



# Safety Processor for the ADAS Domain

Last Updated: Apr 24, 2024

One of the major functions of the AD/ADAS domain controller involve perception and planning. Perception function drives the requirement for very high performance (TOPS) while the subsequent path planning and actuation drives the need for ASIL D safety requirements (DMIPS). ADAS compute may not have ASIL D capabilities, but the ASIL D decision needs to be made in the domain controller. This is achieved by the use of a high-performance ASIL D processor called as safety processor, which acts as a redundant path evaluating the decision made by the ADAS compute.

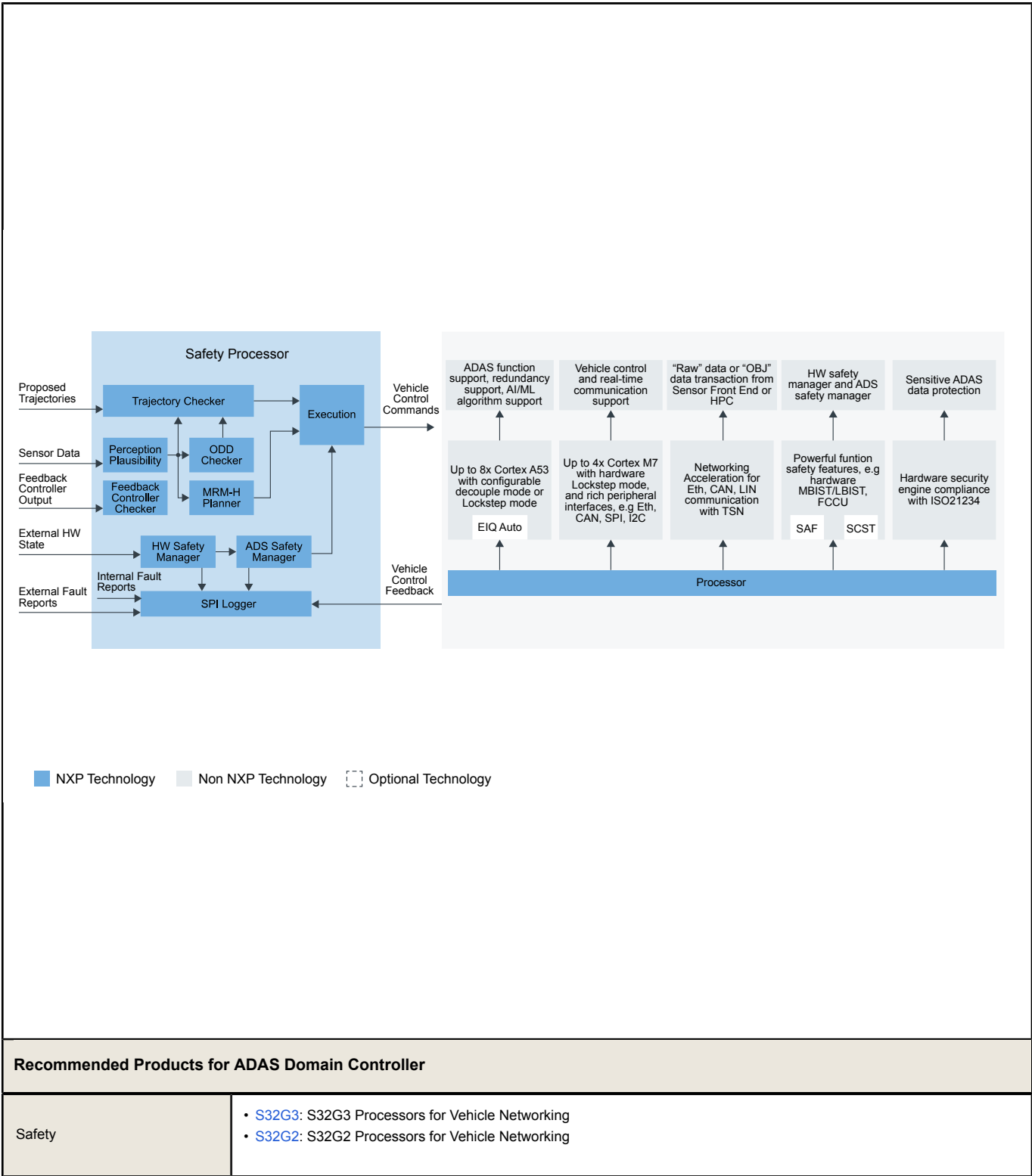
With advancement of ADAS technology, the implemented level of automation driving becomes increasingly higher. However, a degraded mode to keep basic function of ADAS should be supported if any failure leads to complex ADAS application failure. In this situation, a safety processor is needed, which supports powerful function safety features to detect/handle failure and owns enough resource to support degrade/redundancy.

An important feature of ADAS application is that the time-sensitive data or secret data will be transferred between ECU, domain controller and CCU, which drives the requirement that the safety processor in ADAS domain to have excellent networking capabilities for data transactions. It should support processing and forwarding time-sensitive data via time-bounded communication technology, for example, Time-Sensitive-Networking. To protect secret data, accelerated security services based on hardware security engine will be required.

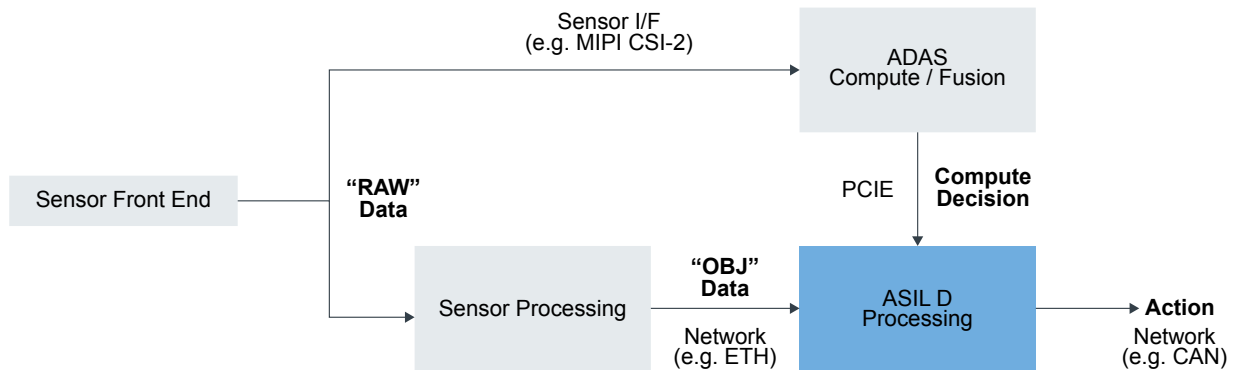
NXP S32G meets all the above-mentioned requirements of ADAS safety co-processor to:

Support ASIL-D applications with powerful function safety features  
Support degraded mode of ADAS  
Support requirements of different ADAS levels  
Provide networking acceleration for CAN and Ethernet with TSN support  
Protect sensitive ADAS data with HSE  
Support high-level OS for SOA applications

## ADAS Domain Controller Block Diagram



**AD / ADS Domain Controller Block Diagram**



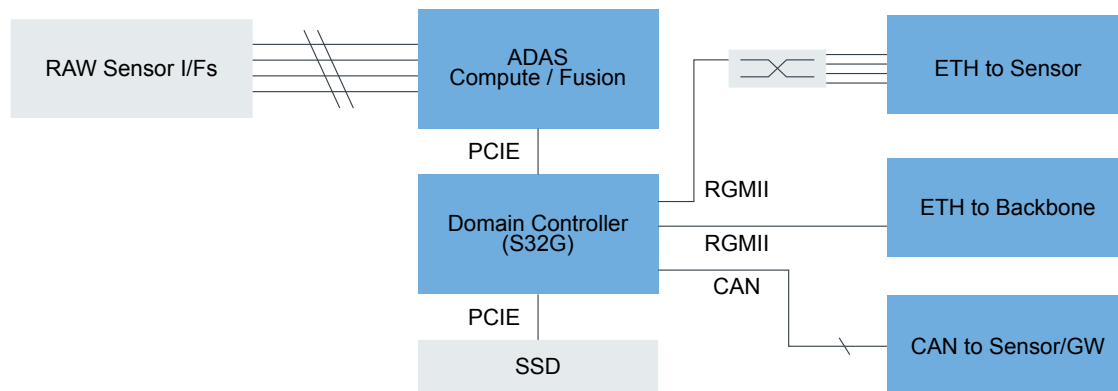
■ NXP Technology   
 ■ Non NXP Technology   
  Optional Technology

**Recommended Products for AD / ADS Domain Controller**

Safety

- [S32G3](#): S32G3 Processors for Vehicle Networking
- [S32G2](#): S32G2 Processors for Vehicle Networking

**ADAS Example Block Diagram**



■ NXP Technology  
 ■ Non NXP Technology  
  Optional Technology

### Recommended Products for ADAS Example

ADAS Compute / Fusion	<ul style="list-style-type: none"> <li>• <a href="#">LX2162A</a>: Layerscape® LX2162A, LX2122A, LX2082A Processors</li> <li>• <a href="#">FS5600</a>: Automotive Dual Buck Regulator and Controller with Voltage Monitors and Watchdog Timer</li> <li>• <a href="#">FS86</a>: Safety System Basis Chip For Domain Controller, Fit For ASIL B and D</li> <li>• <a href="#">LX2160A</a>: Layerscape® LX2160A, LX2120A, LX2080A Processors</li> </ul>
Domain Controller	<ul style="list-style-type: none"> <li>• <a href="#">S32G2</a>: S32G2 Processors for Vehicle Networking</li> <li>• <a href="#">S32G3</a>: S32G3 Processors for Vehicle Networking</li> <li>• <a href="#">PF53</a>: 12 A / 8 A / 15 A Core Supply Regulator with AVP and Watchdog</li> <li>• <a href="#">VR5510</a>: Multi-Channel (9) PMIC for S32G Processor – 8 High Power, 1 Low Power, Fit for ASIL D Safety Level</li> </ul>
Ethernet	<ul style="list-style-type: none"> <li>• <a href="#">TJA1103</a>: TJA1103, ASIL B Compliant Automotive Ethernet 100BASE-T1 PHY Transceiver</li> <li>• <a href="#">TJA1104</a>: TJA1104, MACsec Enabled ASIL B Compliant Automotive Ethernet 100BASE-T1 PHY Transceiver</li> <li>• <a href="#">TJA1120</a>: TJA1120, ASIL B Compliant Automotive Ethernet 1000BASE-T1 PHY Transceiver</li> </ul>

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CAN	<ul style="list-style-type: none"><li>• <a href="#">TJA1463</a>: CAN Signal Improvement Capability Transceiver with Sleep Mode</li><li>• <a href="#">TJA1462</a>: CAN Signal Improvement Capability Transceiver with Standby Mode</li></ul>

View our complete solution for [Safety Processor for the ADAS Domain](#).

**Note:** The information on this document is subject to change without notice.

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