AN12181

Hardware Design Considerations for MKW35A/36A/35Z/36Z Bluetooth Low Energy Devices

Rev. 3 — 10/2019 Application Note

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1 Introduction

This application note describes Printed Circuit Board (PCB) design considerations for the MKW35A, MKW36A, MKW35Z, and MKW36Z 40-pin HVQFN (6 × 6) and 48-pin Laminated QFN (LQFN-7 × 7) package. Included are layouts of the component copper layer, solder mask, and solder paste stencil.

These recommendations are guidelines only and may need to be modified depending on the assembly house used and the other components on the board.

2 QFN component copper layer

2.1 48-pin LQFN

Figure 1 shows a recommended component copper layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the 48-pin LQFN package consists of 48 IC contact pads, and 16 centered ground pads. The copper pattern is as shown in Figure 1.

Use 0.25 mm via holes to connect to the ground plane layers. These are required for RF grounding and help to prevent solder float.

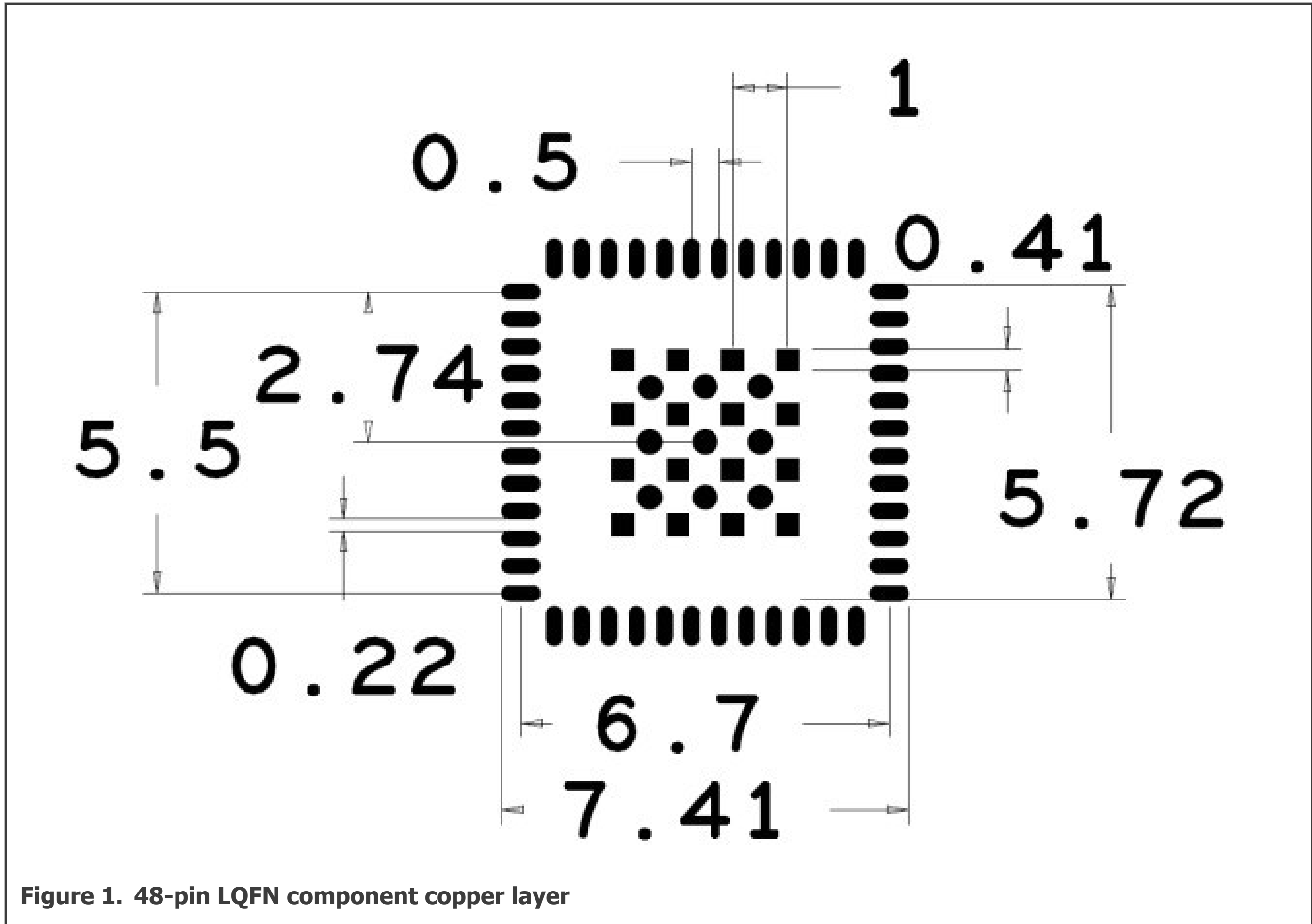

Figure 1. 48-pin LQFN component copper layer

2.1.1 48-pin LQFN solder mask

The solder mask limits the flow of the solder paste during the reflow process. Figure 2 shows a recommended solder mask pattern. The pattern represents openings in the solder mask.

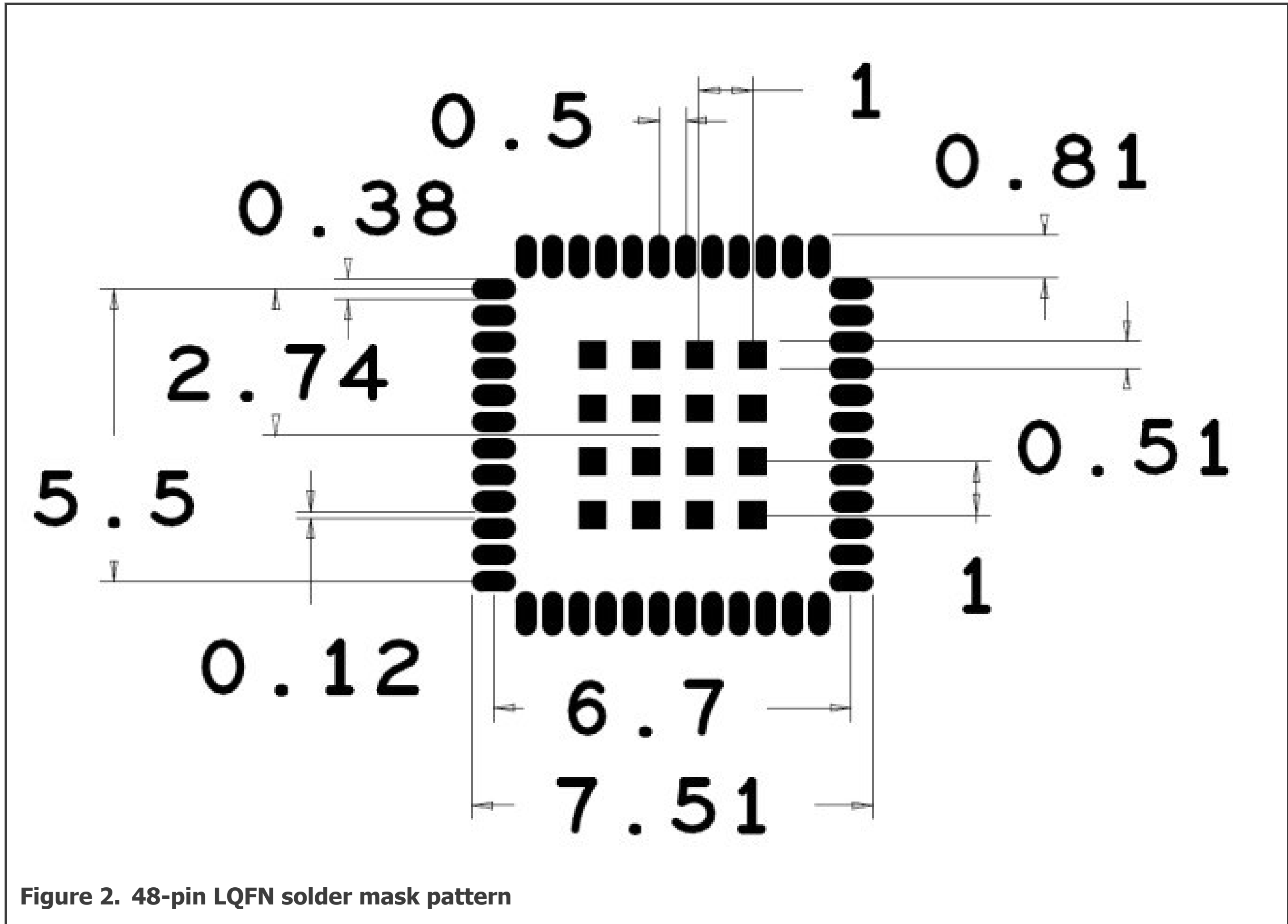

Figure 2. 48-pin LQFN solder mask pattern

2.1.2 48-pin LQFN solder paste stencil

The solder paste stencil controls the pattern and thickness of the solder paste dispensed on the board. Figure 3 shows a recommended solder stencil pattern. Stencil thickness should be approximately 0.1 mm.

Other patterns and opening sizes can be used if too much solder is being applied. See the following section for more information.

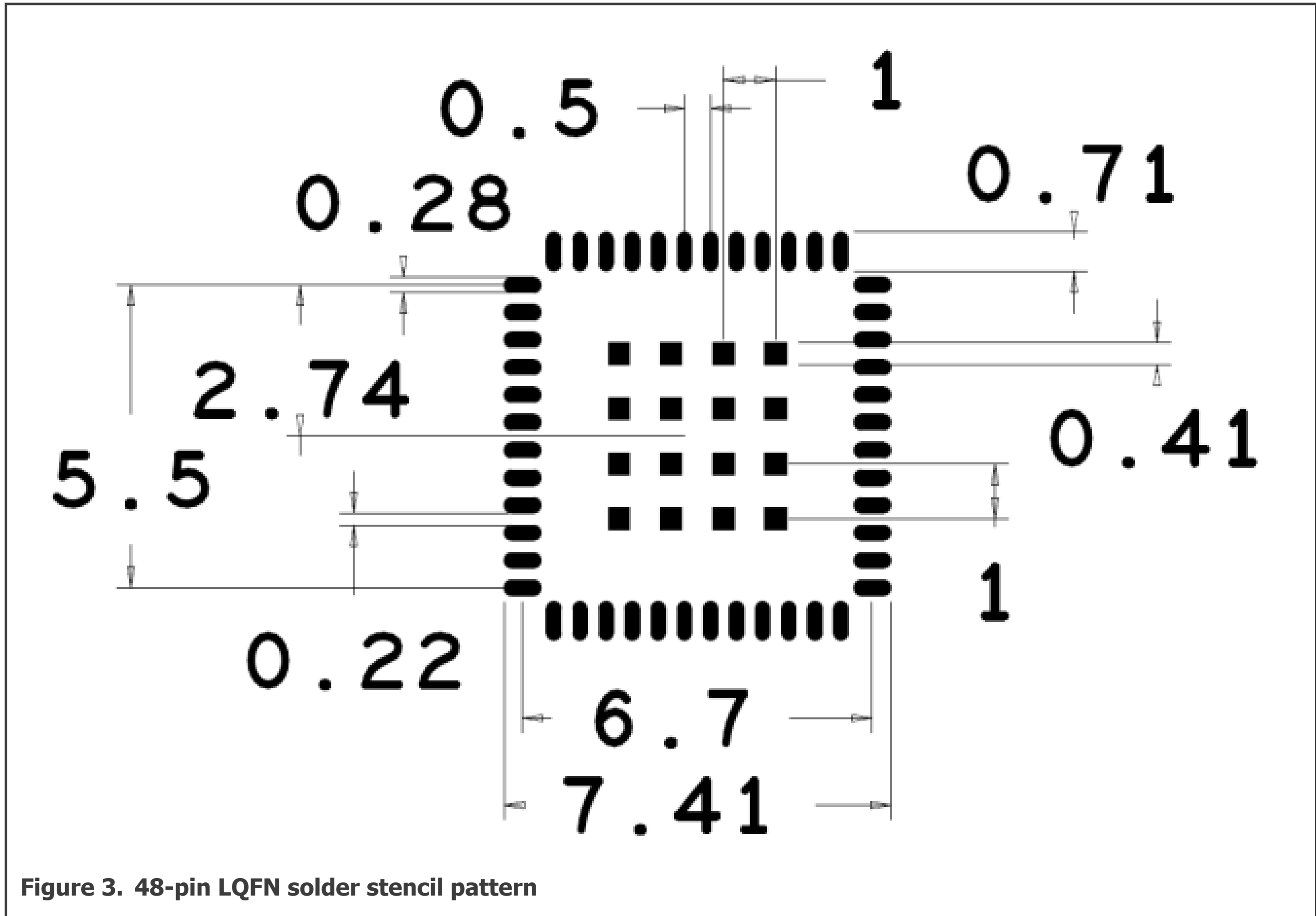

Figure 3. 48-pin LQFN solder stencil pattern

2.2 40-pin HVQFN

Figure 4 shows a recommended component soldering footprint layer. This layer is also referred to as the top metal layer and is the layer to which the components are soldered. The footprint for the 40-pin HVQFN package (6x6) consists of 40 IC contact pads, and 9 centered ground pads. The reflow soldering footprint pattern is as shown in Figure 4.

Use 0.25 mm via holes to connect to the ground plane layers. These are required for RF grounding and help to prevent solder float.

QFN (SAWN), THERMALLY ENHANCED WETTABLE FLANKS,
6 X 6 X 0.85, 0.5 PITCH, 40 I/O

SOT618–13 (DD)

2X 0.575

3X 1.15

0.25

36X 0.5

(40X 0.825)

(80X R)

2X 2.988

3X 1.15

2X 0.575

0.25

(16X 0.95)

PACAKGE OUTLINE

(16X 0.95)

(40X 0.27)

2X 2.988

RECOMMENDED STENCIL THICKNESS 0.125

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

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Figure 4. Reflow soldering footprint for 40-pin HVQFN (SOT618-13)

2.3 LGA problems with excess solder

Excess solder may cause the LGA to float or bridge between the package contacts. To use the correct amount of solder paste applied to the PCB, take into consideration the following:

- Stencil thickness
- Other components mounted on the PCB
- Manufacturing equipment
- Assembly house experience

3 QFN package dimensions

3.1 48-pin

Figure 5 shows the 48-pin LQFN package dimensions.

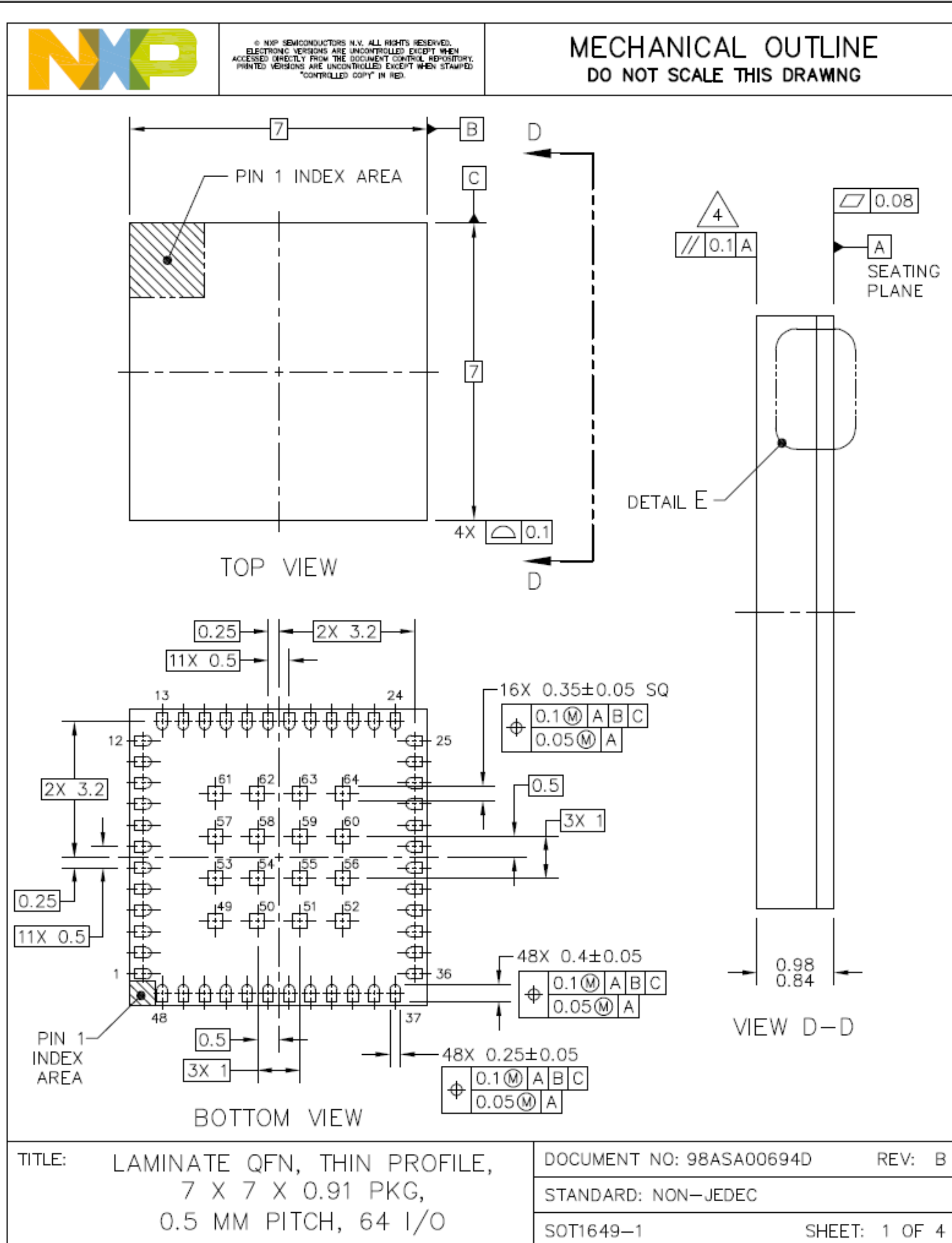

Figure 5. 48-pin LQFN package dimensions

3.1.1 48-pin LQFN device marking details

The MKW35A, MKW36A, MKW35Z and MKW36Z devices are in the 48-pin LQFN (7 × 7 mm). Figure 6 shows device marking examples for the LQFN device.

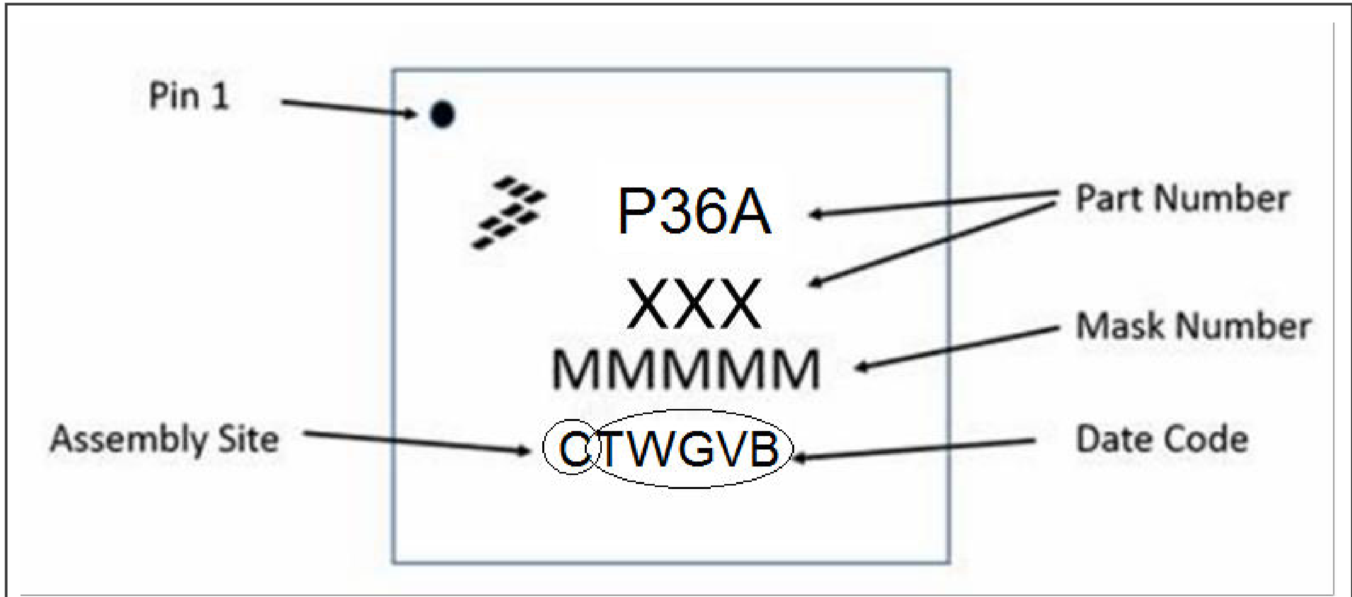

Figure 6. 48-pin LQFN device marking

NOTE

Your device part number may differ from the part number shown in Figure 6.

3.2 40-pin HVQFN

Figure 7 shows the 40-pin HVQFN package dimensions (6 × 6).

QFN (SAWN), THERMALLY ENHANCED WETTABLE FLANKS,
6 X 6 X 0.85, 0.5 PITCH, 40 I/O

SOT618-13 (DD)

TOP VIEW

BOTTOM VIEW

VIEW D–D

DETAIL G

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Figure 7. 40-pin HVQFN package dimensions

3.2.1 40-pin HVQFN device marking details

The MKW35A, MKW36A, MKW35Z and MKW36Z devices are in the 40-pin HVQFN (6 × 6 mm). Figure 8 shows device marking examples for the HVQFN device.

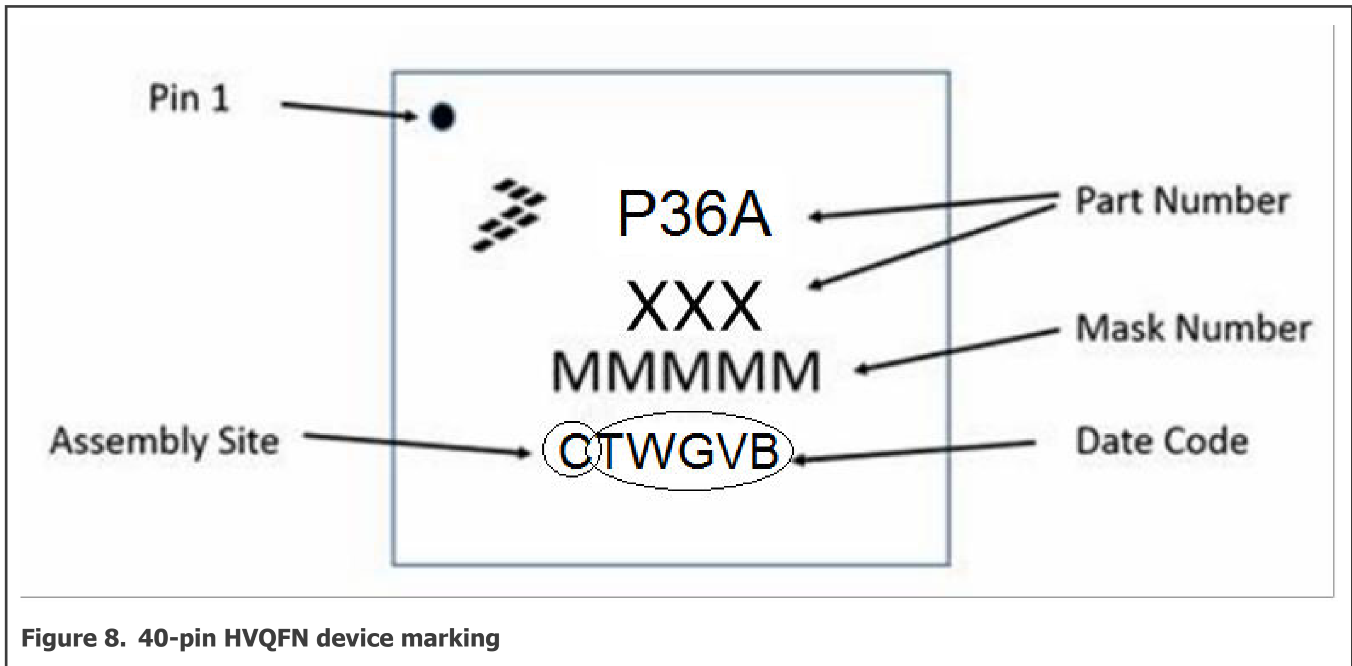

Figure 8. 40-pin HVQFN device marking

NOTE

Your device part number may differ from the part number shown in Figure 8.

4 QFN soldering profile

Figure 9 shows the recommended soldering profile for the MKW36Z HVQFN package, in a board size approximately 3.20 × 2.10 inches.

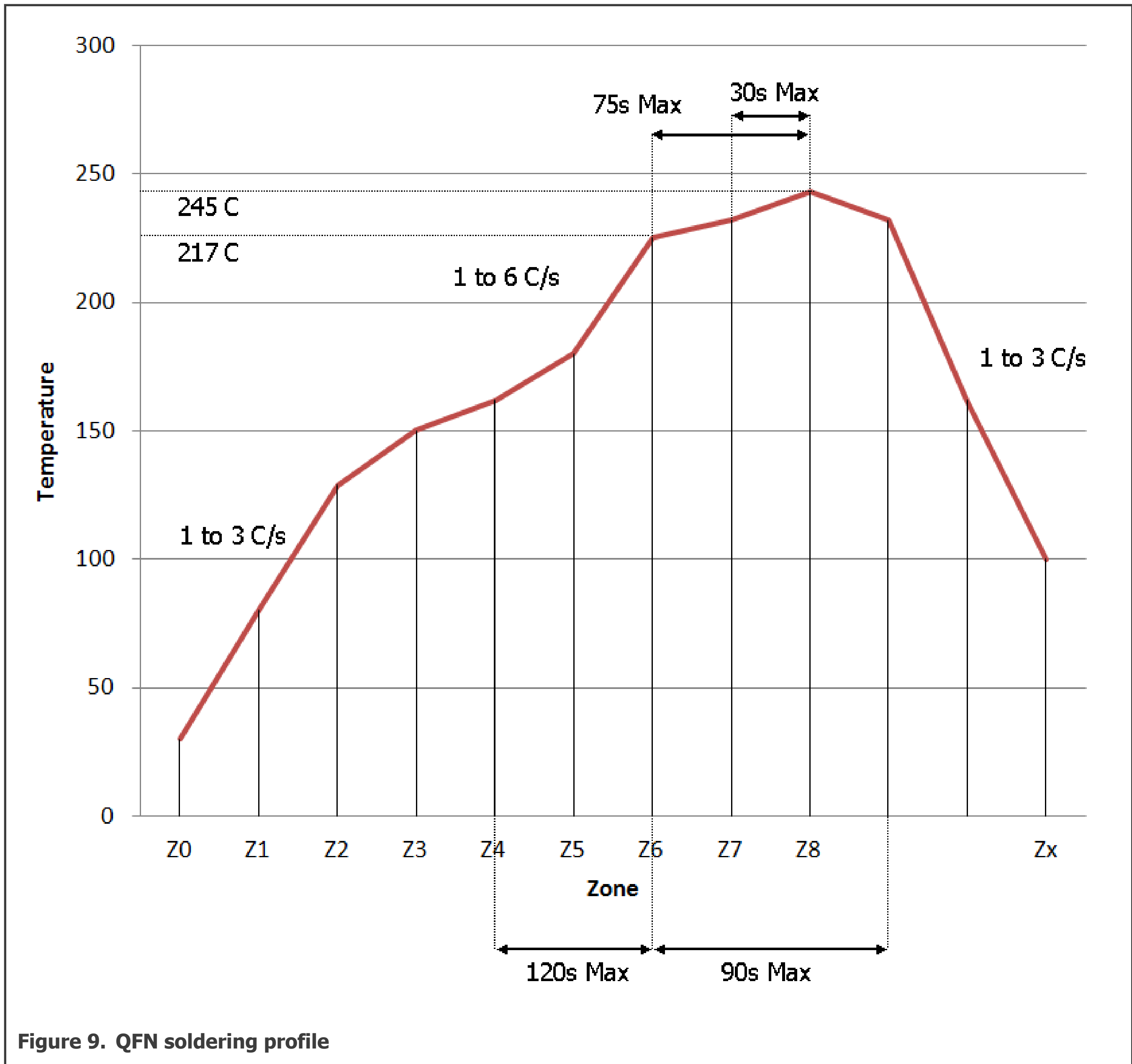

Figure 9. QFN soldering profile

5 Design and board layout considerations

To have successful wireless hardware development, the proper device footprint, RF layout, circuit matching, antenna design, and RF measurement capability are essential. RF circuit design, layout, and antenna design are specialties requiring investment in tools and experience. With available hardware reference designs from NXP, RF design considerations, and the guidelines contained in this application note, hardware engineers can successfully design Bluetooth Low Energy (LE) radio boards with good performance levels. Figure 10 shows the FRDM-KW36 development board. It contains the MKW36Z device and all necessary I/O connections.

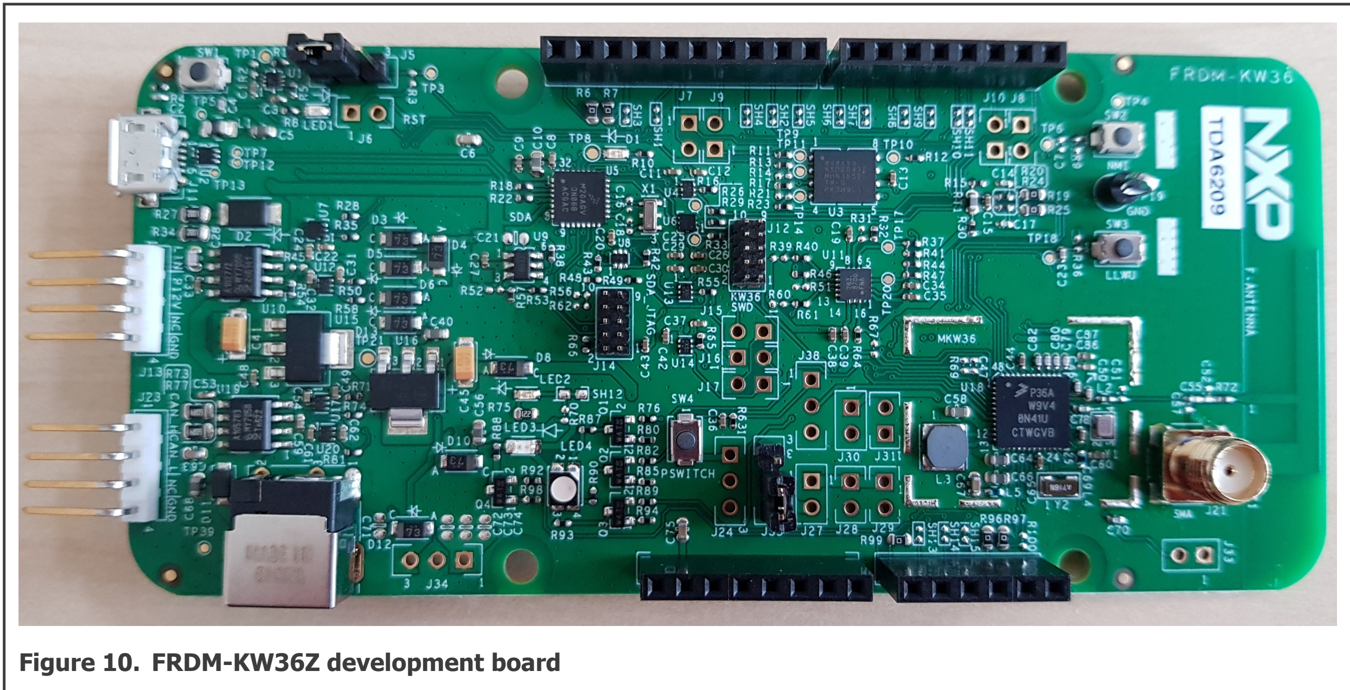

Figure 10. FRDM-KW36Z development board

The device footprint and layout are critical and the RF performance is affected by the design implementation. For these reasons, use of the NXP recommended RF hardware reference designs are important for successful board performance. Additionally, the reference platforms have been optimized for radio performance. If the recommended footprint and design are followed exactly in the RF region of the board; sensitivity, output power, harmonic and spurious radiation, and range will have a high likelihood of first time success.

The following subsections describe important considerations when implementing a wireless hardware design starting with the device footprint, RF circuit implementation, and antenna selection. Figure 11 shows an example of a typical layout with the critical RF section which must be copied exactly for optimal radio performance. The less critical layout area can be modified without reducing radio performance.

NOTE

Exact dimensions are not given in this document, but can be found in the design files for the FRDM-KW36 board.

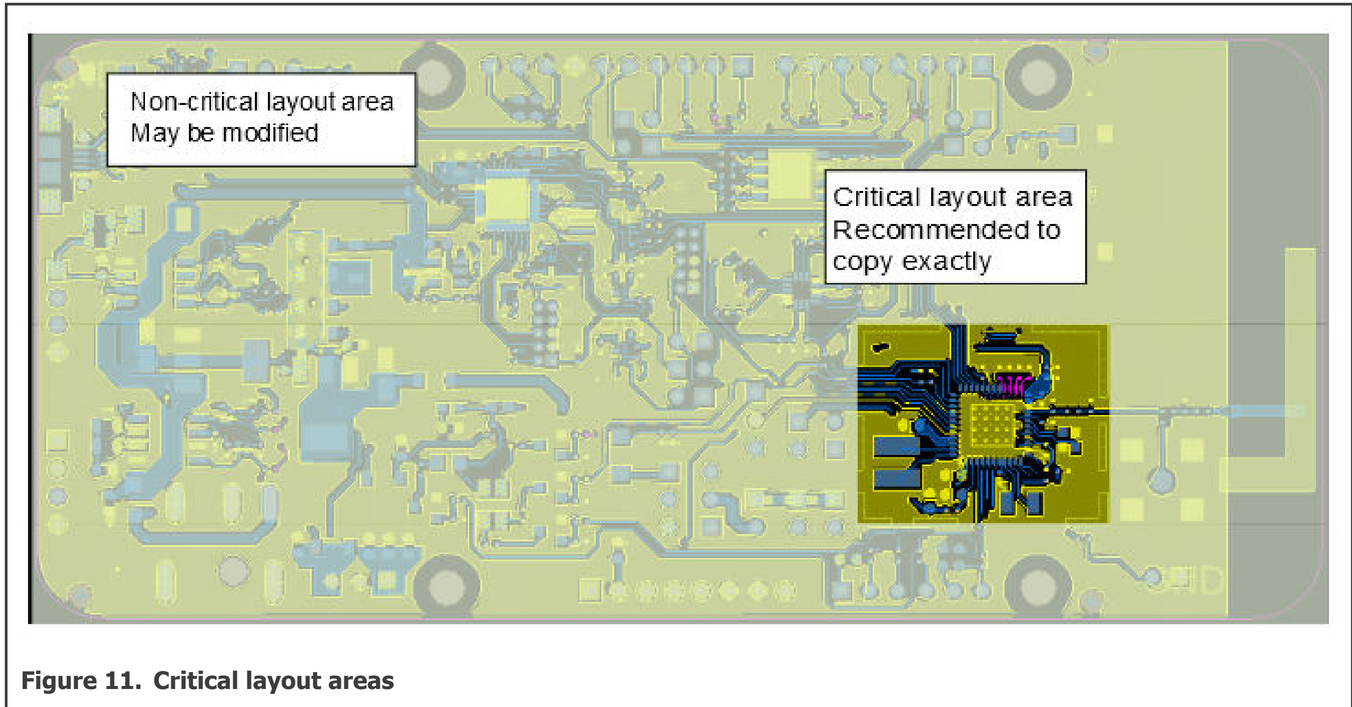

Figure 11. Critical layout areas

5.1 MKW36Z device footprint

The performance of the wireless link is largely influenced by the device's footprint. As a result, a great deal of care has been put into creating a footprint so that receiver sensitivity and output power are optimized to enable board matching and minimal component count. NXP highly recommends copying the die flag exactly as it is shown in Figure 12. It includes via locations as well. Deviation from these parameters can cause performance degradation.

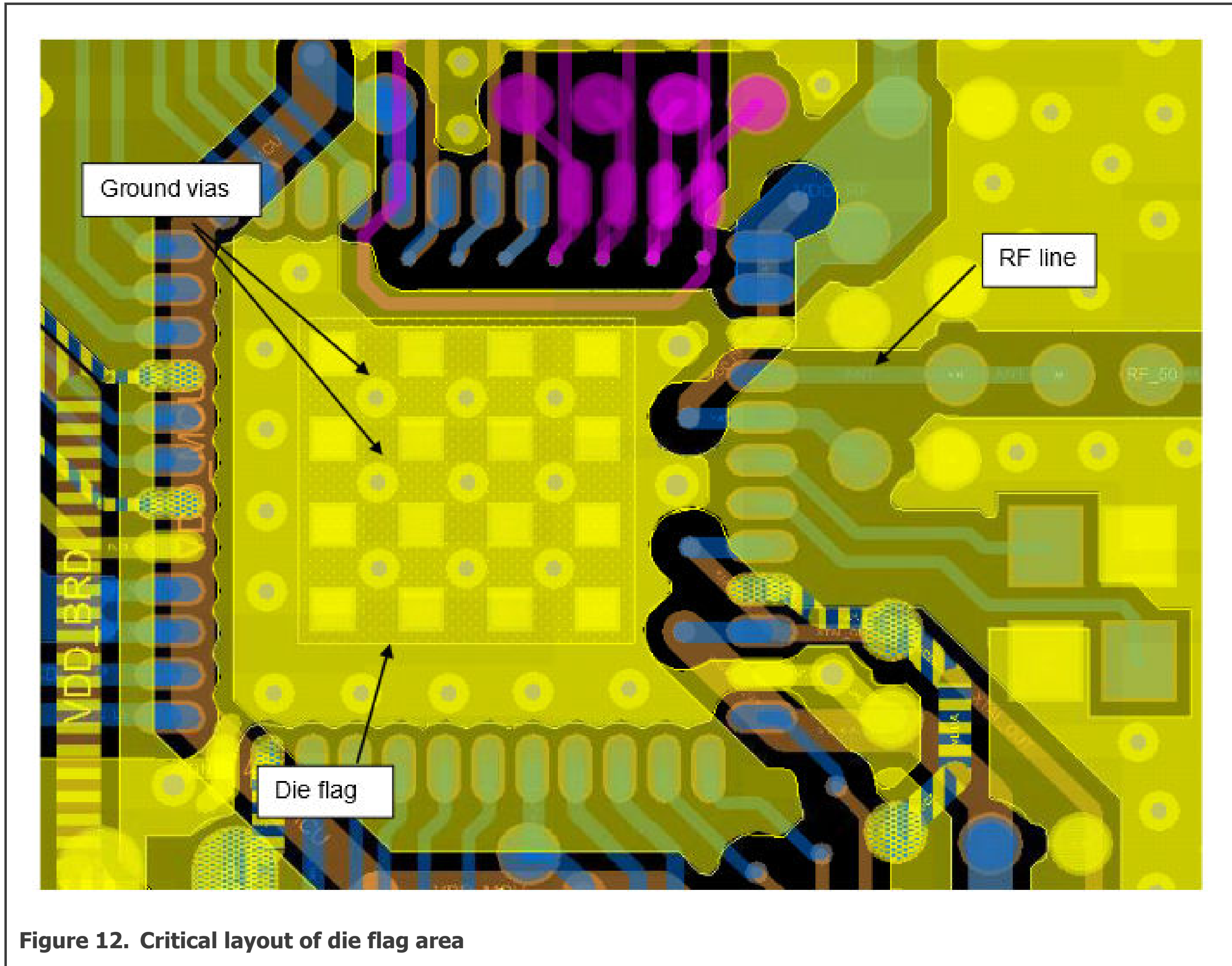

Figure 12. Critical layout of die flag area

Figure 12 shows the critical areas of the device die flag, including:

- Ground vias and locations
- RF output and ground traces
- Die flag shape
- Test pins

As shown in Figure 12, regarding transmission lines, it is important to copy not just the physical layout of the circuit, but also the PCB stackup. Any small change in the thickness of the dielectric substrate under the transmission line will have a significant change in impedance, all this information can be found on the fabrication notes for each board design. As an illustration, consider a 50 ohm trace that is 18 mils wide over 10 mils of FR4. If that thickness of FR4 is changed from 10 to 6 mils, the impedance will only be about 36 ohms.

When the top layer dielectric becomes too thin, the layers will not act as a true transmission line; even though all the dimensions are correct. There is not universal industry agreement on which thickness at which this occurs, but NXP prefers to use a top layer thickness of no less than 8-10 mils. The use of a correct substrate like the FR4 with a dielectric constant of 4.3 will assist you in achieving a good RF design.

Recommendation to reach acceptable EMC during certification:

- A specific attention must be taken on 4 pins PTC1, 2, 3 & 4 if they are used on application.
- Four decoupling capacitors of 3 pF are mandatory on those pins and be positioned closely to the KW36 pins..
- Wires from those 4 pins must be underlayer.
- Vias must be placed under the KW36 package.

Find an example of the recommended layout, as shown in Figure 13.

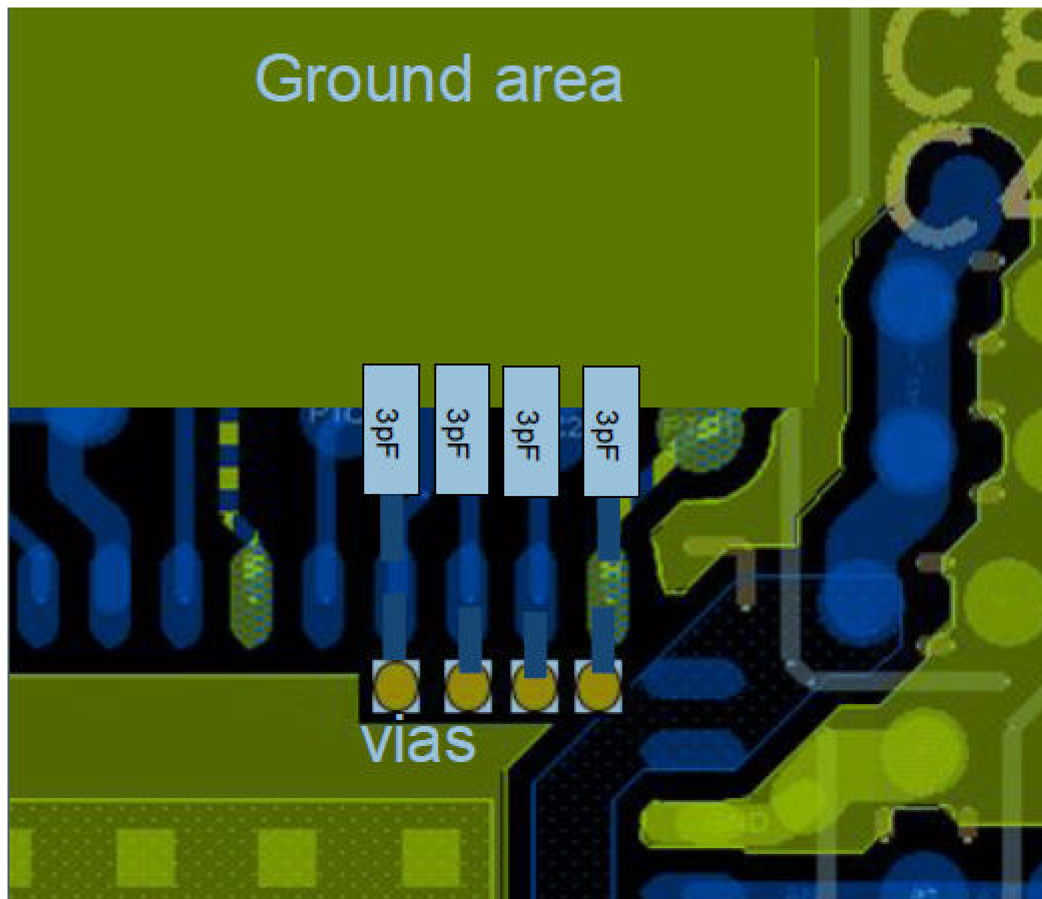

Figure 13. Example of recommended layout

Recommendation to perform a good Vdd_RF supply layout:

- `Vdd_RF1` and `Vdd_RF2` lines must have the same length as possible linked to point A ('Y' connection).
- 12 pF decoupling capacitor from `Vdd_RF` wire must be connected to the Ground Antenna. The purpose is to get the path as short as possible from `Vdd_RF1`/`Vdd_RF2` to the ground antenna
- 12 pF decoupling capacitor from `Vdd_RF3` pin must be as close as possible. Return to ground must be as short as possible. So vias (2 in Figure 14) must be placed near to the decoupling capacitor to get close connection to ground layer.

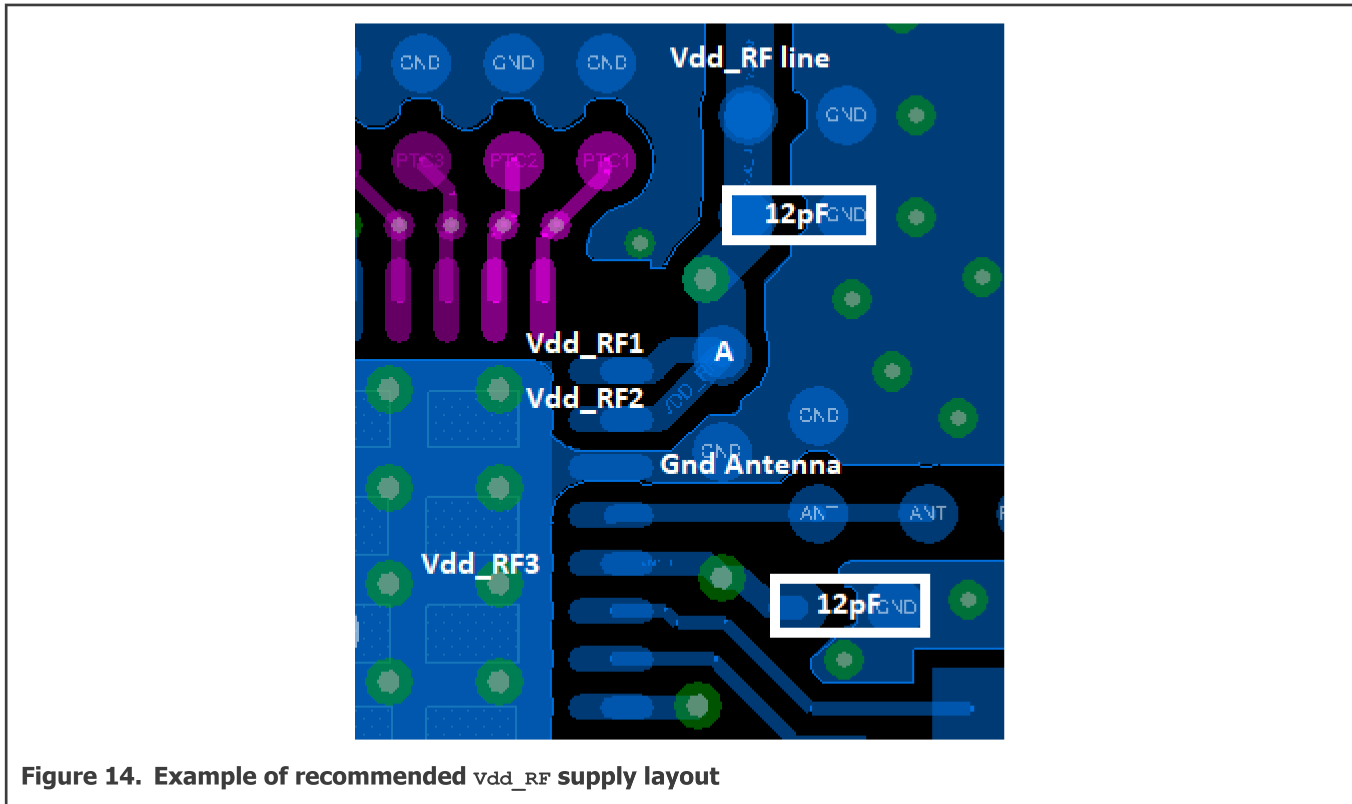

Figure 14. Example of recommended `Vdd_RF` supply layout

5.2 RF circuit topology and matching

Transmission lines have several shapes such as microstrip, coplanar waveguide, and stripline. For Bluetooth LE applications built on FR4 substrates, the types of transmission lines typically take the form of microstrip or coplanar waveguide (CPW). These two structures are defined by the dielectric constant of the board material, trace width, and the board thickness between the trace and the ground.

KW36 has a single ended RF output with a two component matching network composed of a shunt capacitor and a series inductor. These two elements transform the device impedance to 50 ohms. The value of these components may vary depending on your specific board layout. Figure 15 shows the recommended RF-matching network.

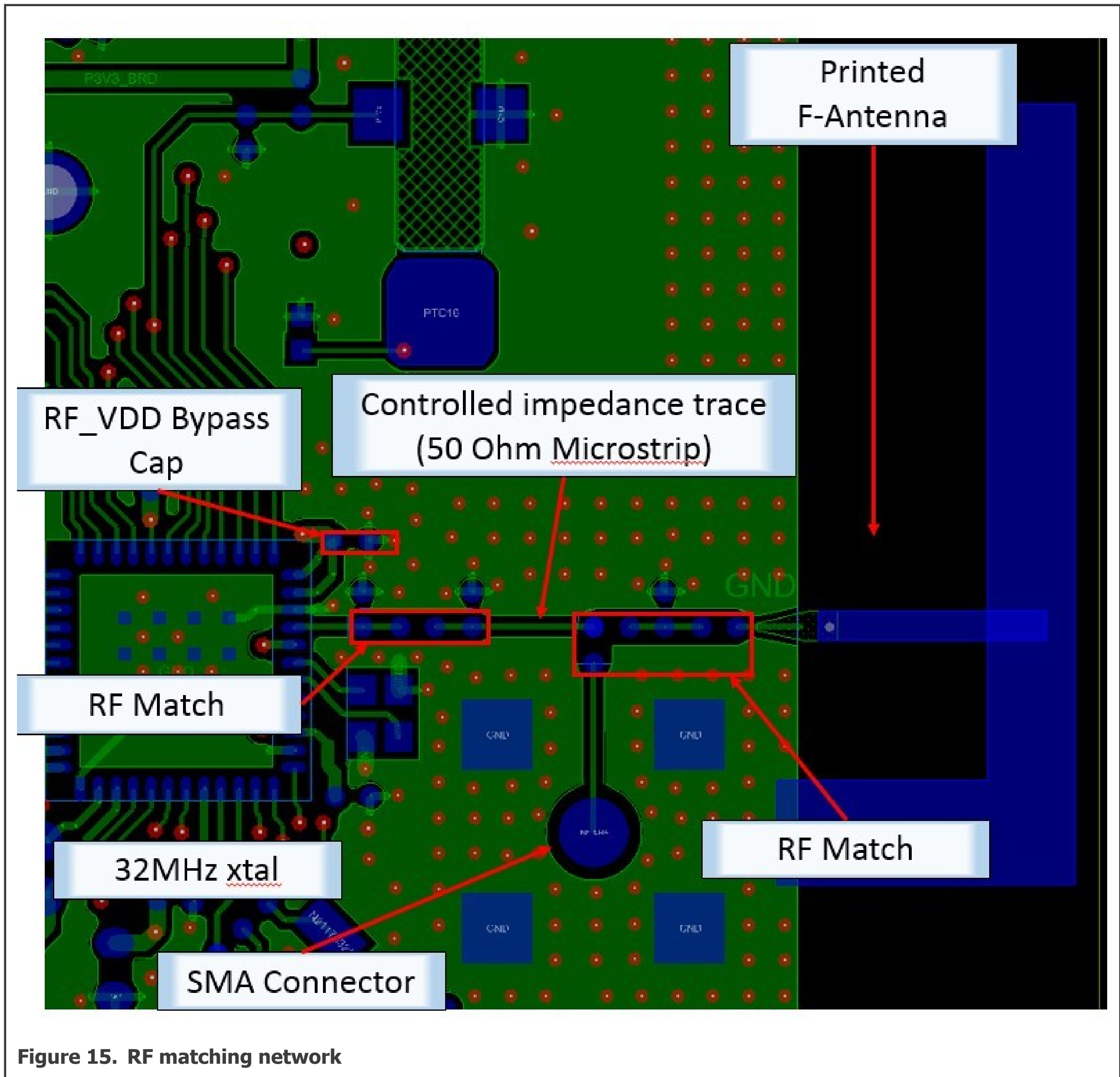

Figure 15. RF matching network

Avoid routing traces near or parallel to RF transmission lines or crystal signals. Maintaining a continuous ground under an RF trace is critical to maintaining the characteristic impedance of that trace. Avoid any routing on the ground layer that will result in disrupting the ground under the RF traces.

Complexity is the main factor that will determine whether the design of an application board can be two- layer, four-layer, or more. The recommended board stackup for either a two-layer or four-layer board design is as follows:

- 2-layer stackup:
  - — Top: RF routing of transmission lines, signals, and ground
  - — Bottom: RF reference ground, signal routing, and general ground
- 4-layer stackup:
  - — Top: RF routing of transmission lines

— L2: RF reference ground

— L3: DC power

— Bottom: signal routing

For more information, see *NXP IEEE 802.15.4 / ZigBee Package and Hardware Layout Considerations* (document ZHDCRM).

5.3 Antenna considerations

There are a large variety of antenna types available to choose from when designing for a wireless system. These include small footprint chip antennas, trace antennas, loop monopole, and dipole, each with their own set of pros and cons depending on the goal of the application. NXP recommends using one of the proven antenna implementations used in many of our hardware reference designs. For more information on compact antenna designs, see *Compact Integrated Antennas* (document AN2731).

Steps for good antenna performance:

- Be mindful of critical dimensions:
  — Critical dimensions should be copied exactly.
  — Customer final board sizes may differ from the NXP reference designs. As a result, the last leg of the trace antenna should be made longer to allow for final board tuning.
  — Antenna tuning may be required to operate at the proper frequency. Ideally, the minimum return loss needs to be centered at 2445 MHz. 10 dB return loss looking into the antenna at the band edges is sufficient to achieve good range and receive sensitivity.
- Antenna impedance is 50 ohm.
  — This is maintained from RF matched port/pin to antenna feed.
  — The example uses microstrip topology but co-planer waveguide with ground can also be used if desired. In this case the dimensions will change so care should be taken when changing from one topology to another.
- The antenna should be reasonably clear of metallic objects and oriented properly with the ground plane.
- Always check the antenna in its final environment, including the PCB, components, case enclosure, hand effects (if appropriate), and battery. Plastic and other materials in the near-field may cause detuning.
- Actual antenna performance can be evaluated in a variety of ways, such as range testing, measuring radiated signal level under controlled conditions, and characteristic testing in an anechoic chamber.

6 Revision history

Table 1. Revision history

Revision number	Date	Substantive changes
3	October, 2019	Recommendation to perform a good `Vdd_RF` supply layout
2	April, 2019	SOT618-13 (iso SOT618-7)
1	December, 2018	Release
0	April, 2018	Initial release

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