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Reference Circuit Design for a SAR ADC in SoC

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1 Introduction

A typical Analog-to-Digital Converter (ADC) compares an input voltage with a reference voltage and generates a digital code corresponding to the input voltage level. Equation 1 on page 1 gives the relation between ADC outputs and input and reference voltage for an ideal SAR ADC. Any kind of disturbance at the reference will have direct impact on the output code. Start-up time, noise, and drive capability are some important characteristics of any reference circuit. This application note discusses each of these characteristics in detail and provides guidelines to achieve the best possible performance from a Successive Approximation Register (SAR) ADC. These recommendations are supported by theory and silicon test data that is collected at Freescale on a bench validation board for the MPC57XX device family. Even though silicon results are shared for a 12-bit, 5 V reference voltage SAR ADC only, the guidelines are applicable for any other SAR ADC evaluation. It is strongly recommended to validate the performance in addition to adhering to the guidelines in this note.

$$ADCOUTPUTCODE = [\frac{V_{IN}}{V_{REF}}]x2^{N}$$

Equation 1

V_{IN}= Analog input voltage

V_{REF}= ADC reference voltage

N= Resolution of ADC

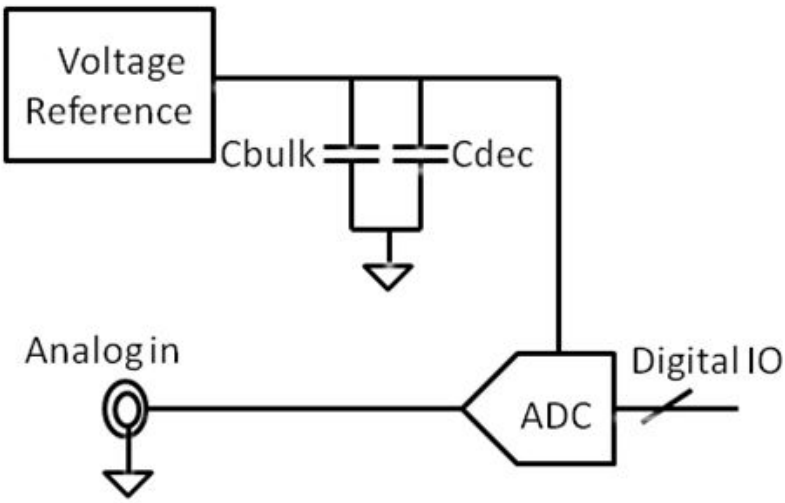

Figure 1. Typical ADC reference circuit

2 Characteristics of reference circuit and their impact on ADC performance

2.1 Start-up time

The time required for the output voltage to reach its final value within a specified error band is defined as start-up time or turn-on time. Start-up time of a voltage reference circuit is a function of output load capacitance and voltage level. Most microcontroller applications may not require continuous operation. There are applications where the ADC circuit will be turned off and will be switched on when required. The on-time of a typical microcontroller while booting from flash will be in the order of 5 ms. The reference voltage circuits should start-up faster than the ADC to provide a stable reference voltage for the ADC to operate. Figure 2 and Figure 3 show the Start-up time profile of slow and fast reference circuits. Figure 4 and Figure 5 show the corresponding ADC output code profile for a DC input. This shows that before the ADC starts conversion, the reference voltage must be stable to get the correct output code.

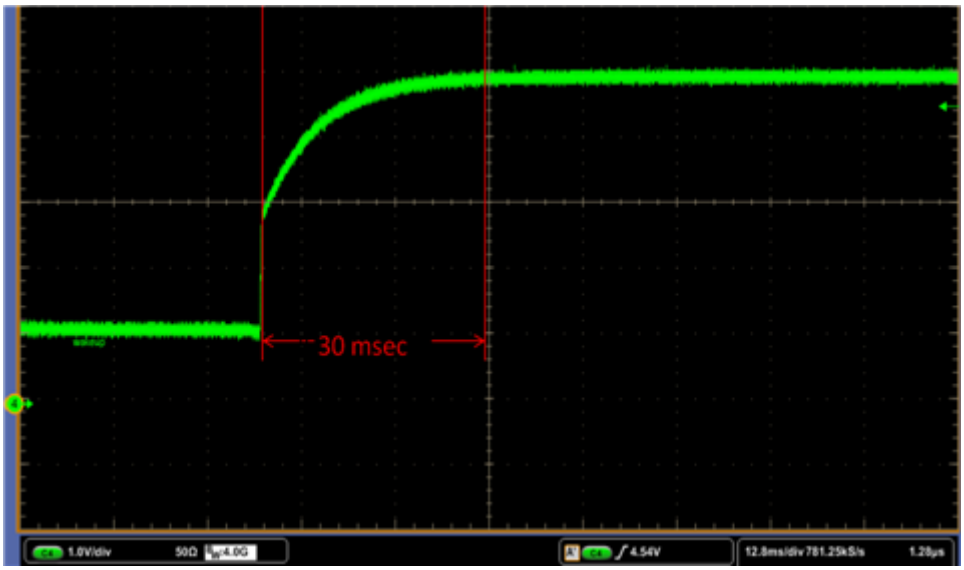

Figure 2. Start-up time profile of slow reference circuit

Figure 3. Start-up time profile of fast reference circuit

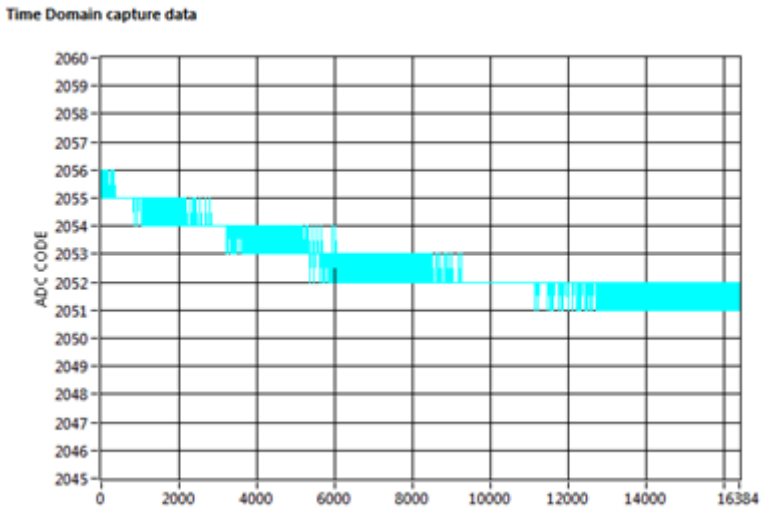

Figure 4. ADC output using slow start-up time reference circuit

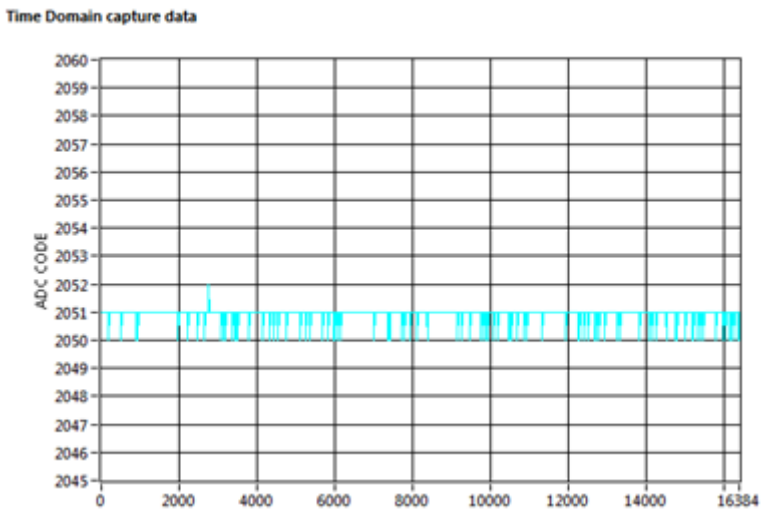

Figure 5. ADC output using fast start-up time reference circuit

2.2 Drive capability

Selection of a reference source depends on the application. Figure 1 shows a typical reference circuit driving a standalone ADC. It consists of a voltage reference source and decoupling capacitors. A voltage reference circuit will have good start-up time but low drive capability in the order of 10 mA to 20 mA. This is sufficient to drive a standalone ADC. However, in an SoC environment, multiple ADC instances may be present. Most of the time, these will share a common reference. In some cases, the supply voltage input and the reference voltage input may even be shorted. Here, an op-amp based buffer circuit can be added between voltage reference and reference pin to meet the load conditions as shown in Figure 6. The voltage reference source and buffer can be replaced with a single linear voltage regulator (LDO). In today's market, a wide range of LDOs are available which have very low noise and fast startup times. Also, some LDOs support an adjustable output voltage which eliminates the need for an additional buffer circuit. Figure 7 shows a Low-dropout (LDO) voltage regulator driving an ADC reference pin. Here, Ro is the equivalent series resistance (sum of output resistance of LDO, trace resistance) between the voltage regulator and the ADC reference pin. This resistance should be low enough such that the voltage drop will be less than 0.5 LSB from the LDO output pin to the ADC reference pin to avoid any conversion errors.

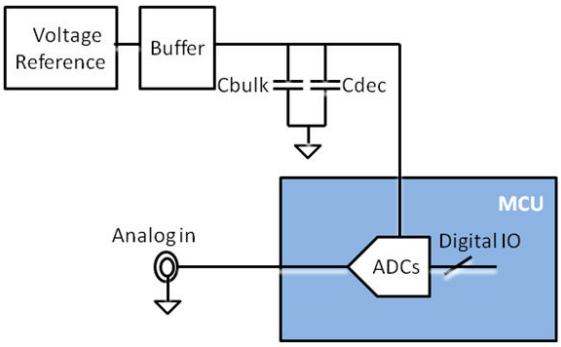

Figure 6. Voltage reference and buffer driving ADCs in SoC

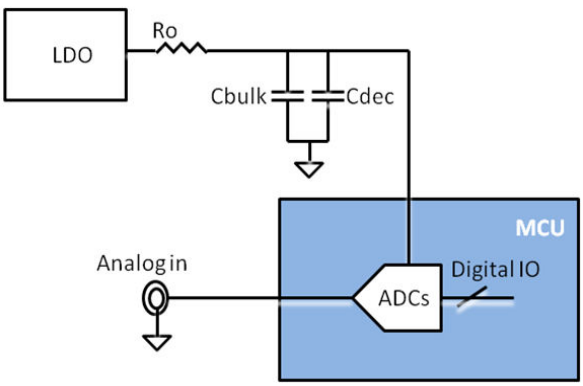

Figure 7. Linear voltage regulator driving ADCs in SoC

2.3 Noise

Common sources of noise are listed below:

- **Ground bounce due to resistance and inductance in the reference path**: Resistance and Inductance in the reference path can be minimized by connecting decoupling capacitors as close as possible to the supply pins and ground planes. The effect of ground bounce in the reference path can be clearly observed when high inductance contactors are used for testing SAR ADCs [2].
- **Interaction of analog and digital switching currents**: A common ground plane is recommended for a typical data converter system. The designer should make sure the analog and digital ground return currents are localized by creating short routes. A well-designed board should have the analog and digital circuits in separate sections of the board (with minimum overlapping).
- **Reference source (LDO noise)**: The reference circuit noise should be at least 10 dB better than the Device Under Test (DUT) [1].

To verify the effect of reference noise two types of reference circuits are selected.

- 50 µV rms noise integrated noise from DC to 100 kHz- will be referred as low noise reference source
- 500 µV rms noise integrated noise from DC to 100 kHz- will be referred as high noise reference source

Figure 8 and Figure 9 show the linearity data collected using a low noise and a high noise reference circuit at the same condition. A Differential Non-Linearity (DNL) flare up at higher codes can be observed with the noisy reference circuit. Figure 10 and Figure 11 show FFT plots collected using low noise and noisy source reference circuits. Figure 12 shows the

low frequency noise profile with zoom for a low noise and noisy source reference circuit. Low frequency noise can be related to the reference circuit noise profile. Given the importance of the quality of the reference source, it is important to pick a good quality source to drive the SAR ADC reference.

If the reference noise level is close to the ADC noise level, a trend may not be visible in static (e.g. DNL) and dynamic (e.g. Signal-to-Noise Ratio (SNR)) plots. However, the ADC can show degradation in the performance numbers. To confirm whether the performance degradation is due to reference noise or not, a simple experiment can be done.

Collect system noise at several values of analog input voltages from 0 to full scale. In this experiment, the input should be relatively low noise as compared to ADC noise. Figure 13 shows the variation of system noise with input voltage for a typical SAR ADC. Here, data is collected with low noise reference and a noisy voltage reference source at the same conditions. Figure 13 clearly shows if the reference circuit noise is relatively low as compared to ADC noise, then the overall system noise (reference noise + ADC noise) is constant, otherwise, it will linearly increase with ADC input [3]. This experiment can be used to find if any reference noise trend exists even in the order of LSBs.

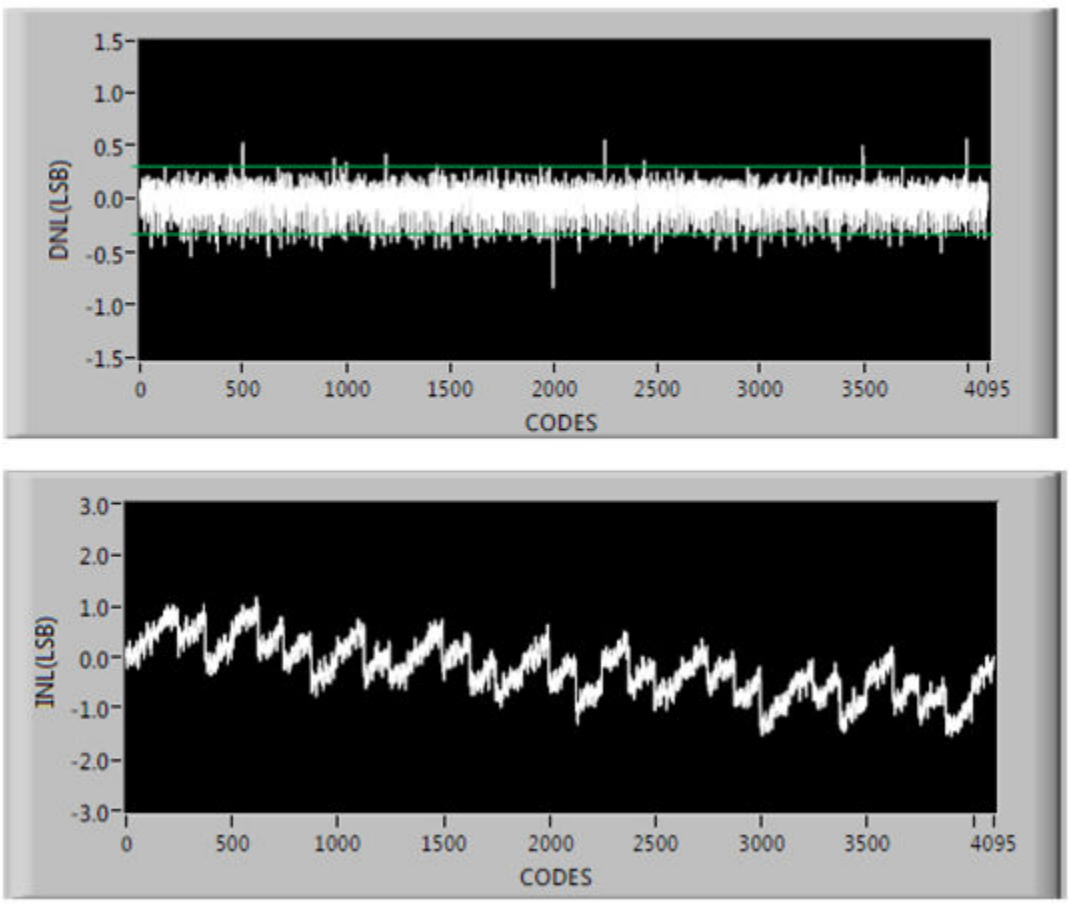

Figure 8. DNL and INL using low noise reference source

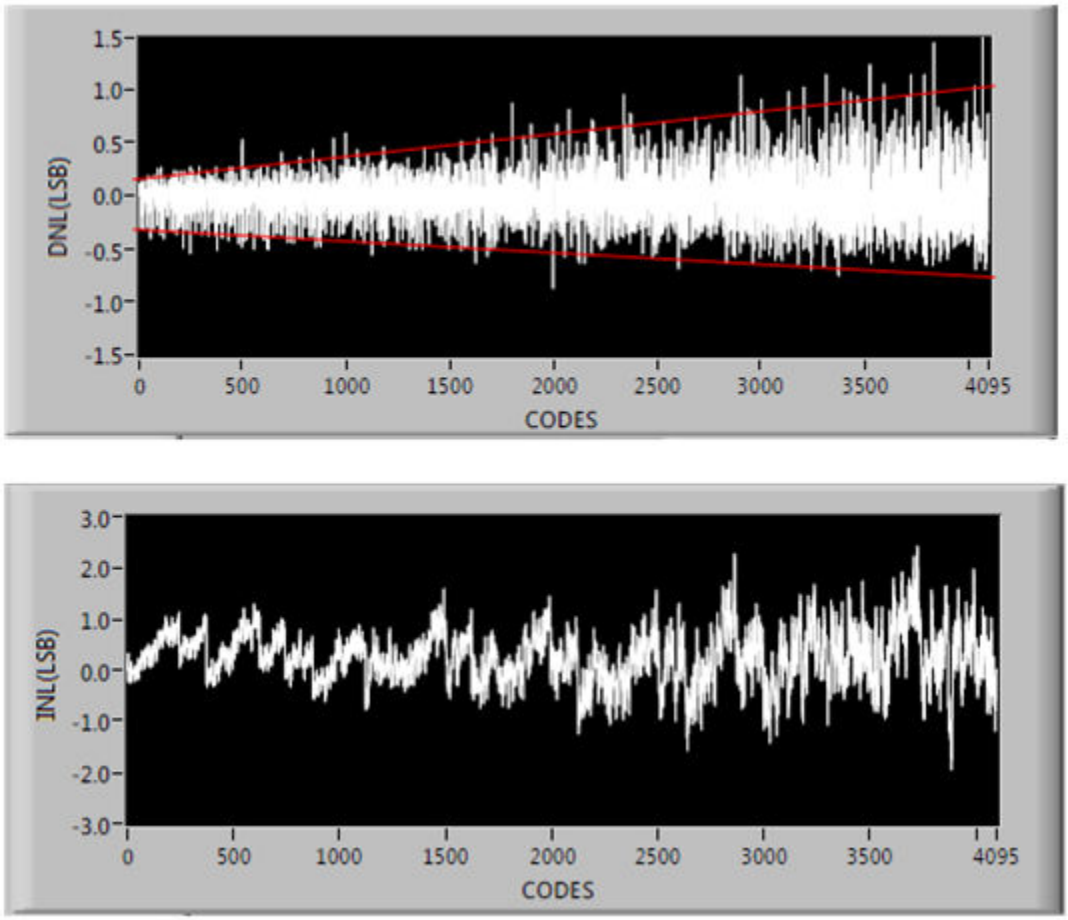

Figure 9. DNL and INL using high noise reference source

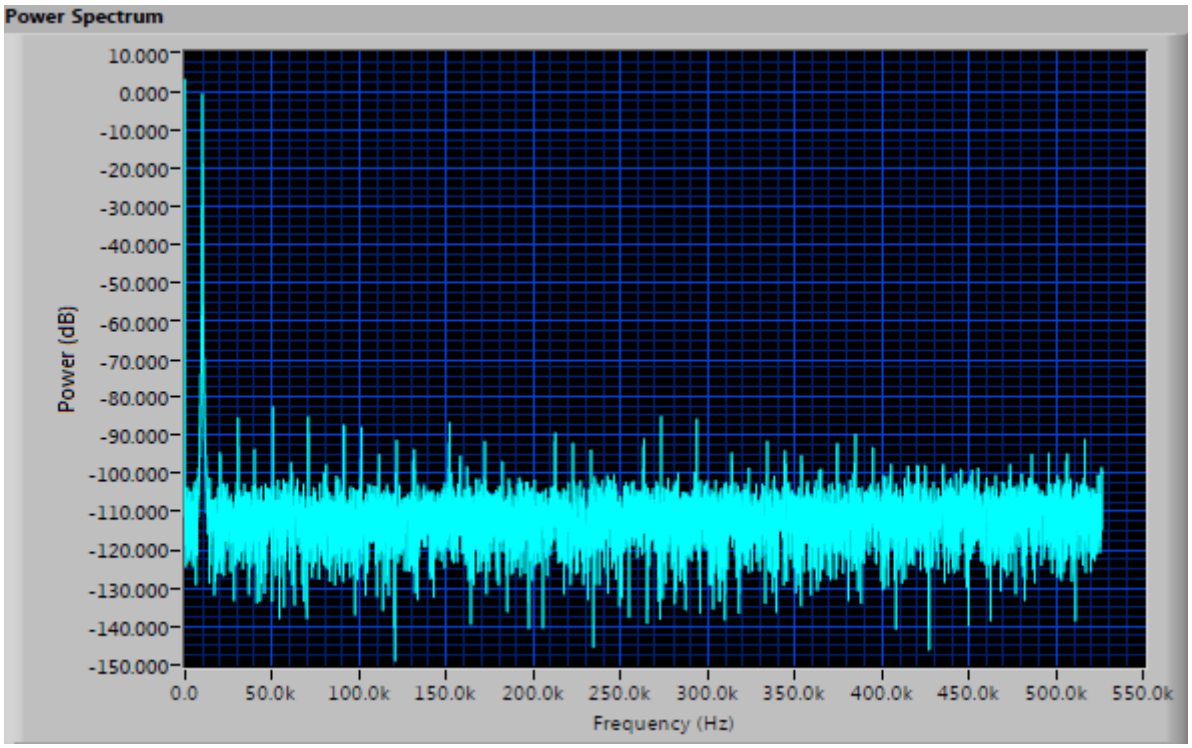

Figure 10. SAR ADC FFT using low noise reference source

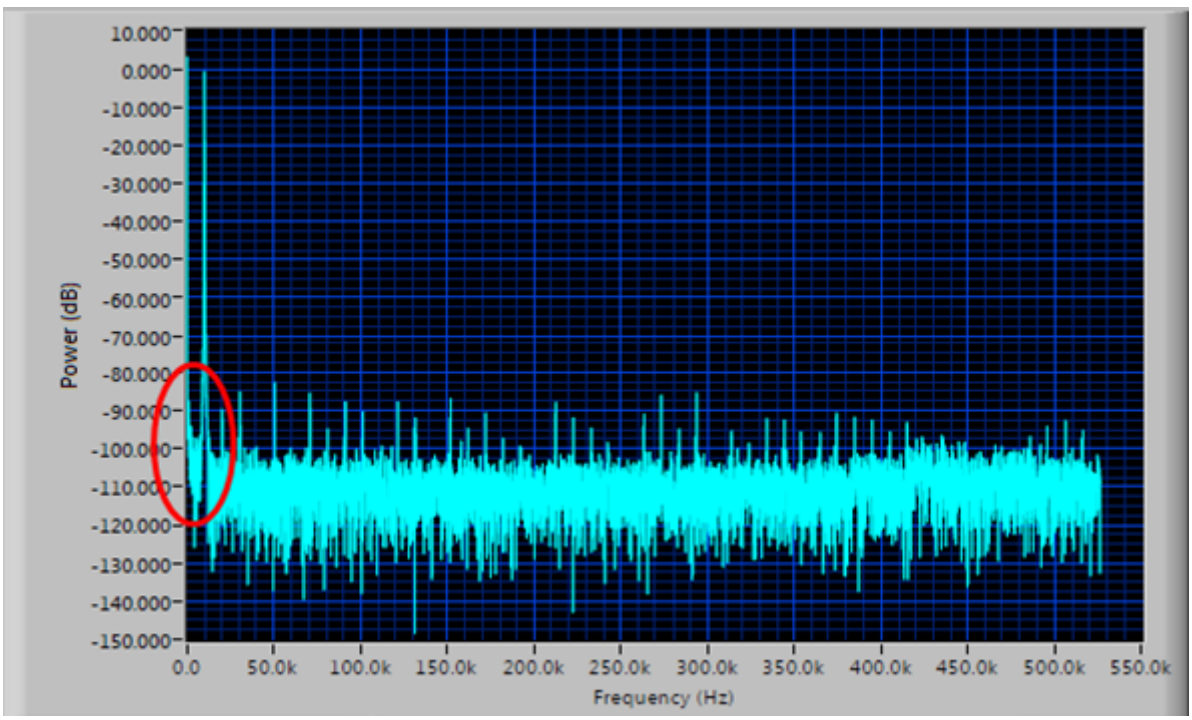

Figure 11. SAR ADC FFT using high noise reference source

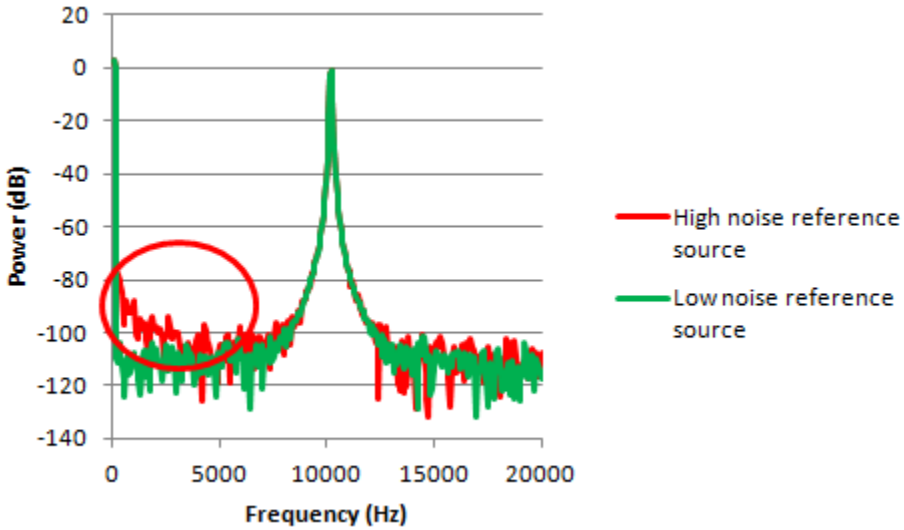

Figure 12. SAR ADC FFT with highlighted low frequency noise

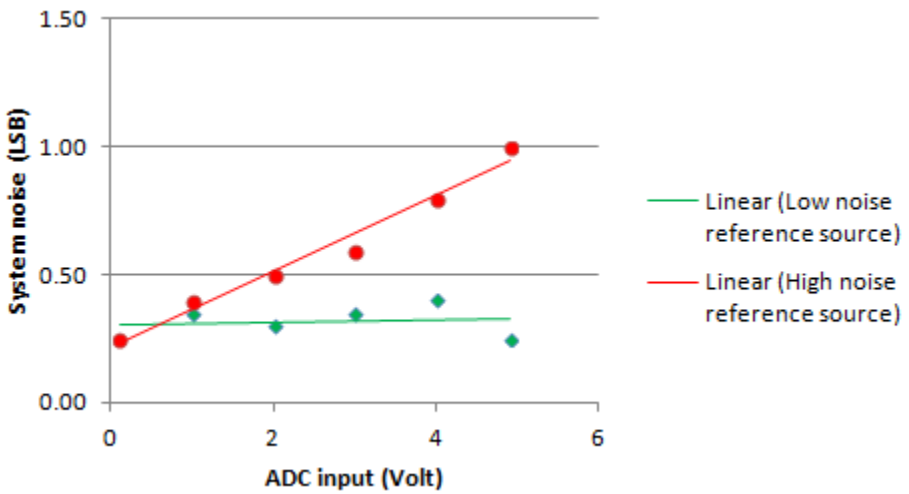

Figure 13. Effect of reference noise on the ADC performance

3 Step-by-step procedure to design a reference circuit

In the previous sections, effect of Start-up time, Noise and importance of Drive capability is discussed. This section provides a step-by-step procedure for designing a SAR ADC reference circuit. Design steps are given for below specifications of a SAR ADC.

Reference voltage, V_{REF}=5.0 V

Average reference current, I_{REF}=100 µA

Resolution, N=12-bit

Step 1: Calculation of maximum allowed series resistance in the reference path:

$$Half\ LSB voltage level, V_{halflsb} = [\frac{1}{2}]x[\frac{V_{REF}}{2^N}]$$

Equation 2

$$V_{halflsb} = 610\,\mu\,V$$

Equation 3

$$R_0 = \frac{V_{half_{lsb}}}{I_{REF}}$$

Equation 4

$$R_o = \frac{610\mu V}{100\mu V} = 6.1\,\Omega$$

Equation 5

Ensure resistance between the reference circuit and the ADC reference pin (sum of LDO output resistance, PCB trace resistance) is less than the above calculated value.

Step 2: Calculation of minimum required decoupling capacitor in the reference path:

For good stability, a regulator datasheet typically recommends a minimum capacitor value at the voltage output pin. Similarly, for SAR ADC, the device documentation contains a recommendation on the minimum value of decoupling capacitors to be used. In such a case, pick the higher of these two so that it meets the requirements of both circuits.

Step 3: Calculation of maximum allowed noise in the reference path:

The reference circuit with decoupling capacitor will form a first order low pass filter. Its noise bandwidth (BW) is given by:

$$NoiseBW = [\frac{1}{2\Pi R_0 C_{eq}}]x\frac{\Pi}{2}$$

Equation 6

$$NoiseBW = \frac{1}{4R_0 C_{eq}}$$

Equation 7

where,

R_0=Total resistance between regulator and reference pin of ADC.

C_{eq}=Total capacitance connected at the ref pin.

Procedure to calculate R_o & C_{eq} is provided in step 1 & 2.

Let's assume these values are as follows:

R_0=0.5 Ω

C_{eq}=4.7 µF + 0.1 µF (bulk & small capacitor)

The noise bandwidth would then be

$$NoiseBW = \frac{1}{4x0.5x4.8E{-}06} = 104.17KHz$$

Equation 8

Generally, LDO datasheets provide noise profile details. One must make sure that the reference circuit noise integrated over the noise BW (as per Equation 7 on page 10) is 10 dB better than the DUT [1].

4 Summary

Startup time, stability, drive capability, and noise are some of the important characteristics which need to be considered while selecting a reference source for a SAR ADC. To get the best dynamic performance, the reference system noise profile should be at least 10 dB better than DUT. The SAR ADC presents a dynamic load, therefore the reference circuit should have good driving capability. With advancement in VLSI technology, low noise and startup time LDOs available in the market provide a good fit for driving multiple high resolution SAR ADCs.

5 References

1. AN4881: *MPC57xx SAR ADC Implementation and Use*, available at freescale.com .
2. Maugard, G., C. Wegneer, T. O'Dwye, M.P. Kennedy. "Method of reducing contactor effect when testing high-precision ADCs," Test Conference, 2003, Proceedings, ITC 2003.
3. Oljaca, M., W. Klein. "Converter voltage reference performance improvement secrets," Instrumentation & Measurement Magazine, IEEE, Volume: 12, Issue: 5 October 2009.

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