

Migrating between MPC5748G and MPC5746C

by: Chris Platt

1. Introduction

This document is intended to help users migrate between the MPC5748G and MPC5746C microcontroller devices by outlining the important differences between them. Both MPC5748G and MPC5746C processors are part of the next generation automotive body microcontrollers aimed at body and gateway applications. While both devices are suitable for the same applications and even though they are both based on the same technology and architecture, there are some differences the user must be aware of when migrating an application from one device to another.

The MPC5748G device offers microcontrollers with more features and processing power than the MPC5746C. This makes the MPC5748G device ideal for the most demanding applications in terms of processing power, communication alternatives, and overall data throughput. On the other hand, the MPC5746C has a more specific set of peripherals tailored for applications that require less processing power or where the MPC5748G's features would be excessive (and costly).

This application note is divided into four large sections

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General differences

that cover the following areas:

- General differences
- Hardware differences
- Booting differences
- Peripheral difference

Please note that this document is a guideline of the differences between the MPC5748G and MPC5746C devices and is not an extensive overview. It is recommended that this document is read along with the reference manuals of each device where these differences are reviewed in detail. The reference manuals and datasheets can be found at freescale.com.

2. General differences

Even though the MPC5748G and MPC5746C were designed with the same architecture and peripherals, there are important differences to consider when migrating from one device to the other. As mentioned earlier, the MPC5748G has a richer feature set than the MPC5746C, the user must ensure that the MPC5746C can still meet the application requirements before considering migrating from one device to another. The table below condenses the main differences between the two devices.

Table 1. **General differences between the MPC5748G and MPC5746C devices**

MPC5748G	MPC5746C
2 x e200Z4 cores	1 x e200z4 core
6 MB flash memory (triple ported)	3 MB flash memory (dual ported)
768 KB SRAM memory (three arrays)	384 KB SRAM memory (two arrays)
2 XBAR Switches	1 XBAR Switch
6 SPI modules	4 SPI modules
18 LinFlex modules	16 LinFlex modules
1 USB_Host + 1 USB_OTG modules	No USB support
2 ENET modules	1 ENET module
L2 Ethernet switch	No Ethernet Switch
uSDHC module	No uSDHC support
MLB150 module	No MLB support
3 STM modules	2 STM modules
4 SWT modules	3 SWT modules

MPC5748G	MPC5746C
3 eMIOS modules	2 eMIOS modules
5 DSMC modules	4 DSMC modules
2 SMPU module	1 SMPU module
2 DMAMUX	1 DMAMUX
No Glitch Filter support	Glitch Filter support

Please refer to “[Peripheral differences](#)” for more information on the impact that each of these differences have on an application developed for the MPC5748G that needs to be migrated to the MPC5746C device.

3. Hardware differences

Both devices offer the same three package options (176 LQFP, 256 MAPBGA, and 324 MAPBGA) and are pin to pin compatible on most applications. This section details the specific pins whose functions change between devices.

3.1. Pinouts

Here is a detailed list of the functionalities that are different between the MPC5748G and the MPC5746C. Please note that the MPC5746C has fewer peripherals so the pins that have those functionalities on the MPC5748G no longer do. This is the reason this list may seem quite extensive.

Table 2. **Function comparison between MPC5748G and MPC5746C**

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PA[2]	2	0000_0010	E2UC_0_X		O	17	F1	J6	Removed
PA[2]	584	0000_0010	E2UC_0_X		I	17	F1	J6	Removed
PA[4]	4	0000_0011	E2UC_24_X	E0UC_24_X	O	51	T2	P6	Changed
PA[4]	536	0000_0101		E0UC_24_X	I	51	T2	P6	Added
PA[4]	608	0000_0010	E2UC_24_X		I	51	T2	P6	Removed
PA[5]	5	0000_0100	ULPIO_STP		O	146	C10	A14	Removed
PA[6]	745	0000_0001	ULPIO_DIR		I	147	D11	A13	Removed
PA[10]	10	0000_0100	MII_1_TXD[1]		O	131	A15	D18	Removed
PA[11]	11	0000_0011	MII_1_TXD[0]		O	132	B14	D17	Removed
PA[11]	766	0000_0001	ULPIO_FAULT		I	132	B14	D17	Removed
PA[12]	1018	0000_0001		INP (GF)	I	53	P6	N8	Added

Hardware differences

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PA[12]	12	0000_0011	E2UC_26_Y	E0UC_26_Y	O	53	P6	N8	Changed
PA[12]	538	0000_0100		E0UC_26_Y	I	53	P6	N8	Added
PA[12]	610	0000_0010	E2UC_26_Y		I	53	P6	N8	Removed
PA[13]	1018	0000_0011		INP (GF)	I	52	R5	P7	Added
PA[13]	13	0000_0011	E2UC_25_Y	E0UC_25_Y	O	52	R5	P7	Changed
PA[13]	537	0000_0100		E0UC_25_Y	I	52	R5	P7	Added
PA[13]	609	0000_0010	E2UC_25_Y		I	52	R5	P7	Removed
PA[14]	14	0000_0100	E2UC_23_X	E0UC_23_X	O	50	P4	T3	Changed
PA[14]	535	0000_0101		E0UC_23_X	I	50	P4	T3	Added
PA[14]	607	0000_0010	E2UC_23_X		I	50	P4	T3	Removed
PA[15]	15	0000_0100	E2UC_21_Y	E0UC_21_Y	O	48	R2	N7	Changed
PA[15]	533	0000_0011		E0UC_21_Y	I	48	R2	N7	Added
PA[15]	605	0000_0010	E2UC_21_Y		I	48	R2	N7	Removed
PB[0]	1019	0000_0001		INP (GF)	I	39	L3	N1	Added
PB[0]	16	0000_0100	E2UC_4_Y	E0UC_4_G	O	39	L3	N1	Changed
PB[0]	516	0000_0101		E0UC_4_G	I	39	L3	N1	Added
PB[0]	588	0000_0010	E2UC_4_Y		I	39	L3	N1	Removed
PB[1]	1019	0000_0100		INP (GF)	I	40	M2	N2	Added
PB[1]	17	0000_0010	E2UC_5_Y	E0UC_5_G	O	40	M2	N2	Changed
PB[1]	517	0000_0100		E0UC_5_G	I	40	M2	N2	Added
PB[1]	589	0000_0010	E2UC_5_Y		I	40	M2	N2	Removed
PB[2]	1019	0000_0010		INP (GF)	I	176	A2	G9	Added
PB[2]	18	0000_0100	SD_DAT7		O	176	A2	G9	Removed
PB[2]	989	0000_0001	SD_DAT7		I	176	A2	G9	Removed
PB[3]	1019	0000_0101		INP (GF)	I	1	D4	G8	Added
PB[3]	19	0000_0011	E2UC_8_X	E0UC_8_X	O	1	D4	G8	Changed
PB[3]	520	0000_0011		E0UC_8_X	I	1	D4	G8	Added
PB[3]	592	0000_0010	E2UC_8_X		I	1	D4	G8	Removed
PB[3]	766	0000_0010	ULPIO_FAULT		I	1	D4	G8	Removed
PB[5]	977	0000_0010	MII_1_RX_DV		I	91	N13	R14	Removed
PB[6]	976	0000_0010	MII_1_RXD[3]		I	92	N14	N12	Removed
PB[7]	975	0000_0010	MII_1_RXD[2]		I	93	R16	P14	Removed
PB[10]	26	0000_0101	E2UC_29_Y	E0UC_29_Y	O	62	N7	P9	Changed
PB[10]	541	0000_0100		E0UC_29_Y	I	62	N7	P9	Added
PB[10]	613	0000_0101	E2UC_29_Y		I	62	N7	P9	Removed
PB[11]	971	0000_0010	MII_1_RX_CLK		I	96	M13	P13	Removed
PB[12]	28	0000_0100	ENET1_TMRO		O	101	L14	N13	Removed
PB[12]	845	0000_0001	ENET1_TMRO		I	101	L14	N13	Removed

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PB[13]	977	0000_0001	MII_1_RX_DV		I	103	L15	T18	Removed
PB[14]	975	0000_0001	MII_1_RXD[2]		I	105	K15	R17	Removed
PB[15]	1019	0000_0001	MLBSIG		I	107	K16	R18	Removed
PB[15]	31	0000_0011	MLBSIG		O	107	K16	R18	Removed
PB[15]	973	0000_0001	MII_1_RXD[0]		I	107	K16	R18	Removed
PC[2]	34	0000_0011	E2UC_22_X		O	145	B11	C13	Removed
PC[2]	606	0000_0010	E2UC_22_X		I	145	B11	C13	Removed
PC[2]	755	0000_0001	ULPI1_CLK		I	145	B11	C13	Removed
PC[3]	35	0000_0011	E2UC_23_X		O	144	C11	D11	Removed
PC[3]	607	0000_0011	E2UC_23_X		I	144	C11	D11	Removed
PC[3]	756	0000_0001	ULPI1_DIR		I	144	C11	D11	Removed
PC[4]	1021	0000_0101		INP (GF)	I	159	A9	B12	Added
PC[4]	36	0000_0011	SD_DAT0		O	159	A9	B12	Removed
PC[4]	36	0000_0100	ULPI0_D1		O	159	A9	B12	Removed
PC[4]	748	0000_0001	ULPI0_D1		I	159	A9	B12	Removed
PC[4]	982	0000_0001	SD_DAT0		I	159	A9	B12	Removed
PC[5]	37	0000_0011	E2UC_24_X		O	158	B9	A11	Removed
PC[5]	37	0000_0101	SD_CLK		O	158	B9	A11	Removed
PC[5]	37	0000_0110	ULPI0_D0		O	158	B9	A11	Removed
PC[5]	608	0000_0011	E2UC_24_X		I	158	B9	A11	Removed
PC[5]	747	0000_0001	ULPI0_D0		I	158	B9	A11	Removed
PC[5]	990	0000_0010	SD_CLK		I	158	B9	A11	Removed
PC[6]	1020	0000_0001		INP (GF)	I	44	N3	R3	Added
PC[6]	38	0000_0011	E2UC_17_Y	E0UC_17_Y	O	44	N3	R3	Changed
PC[6]	529	0000_0011		E0UC_17_Y	I	44	N3	R3	Added
PC[6]	601	0000_0010	E2UC_17_Y		I	44	N3	R3	Removed
PC[7]	1020	0000_0100		INP (GF)	I	45	N4	U2	Added
PC[7]	39	0000_0011	E2UC_18_Y	E0UC_18_Y	O	45	N4	U2	Changed
PC[7]	530	0000_0011		E0UC_18_Y	I	45	N4	U2	Added
PC[7]	602	0000_0010	E2UC_18_Y		I	45	N4	U2	Removed
PC[8]	40	0000_0011	SD_DAT6		O	175	B3	D5	Removed
PC[8]	988	0000_0001	SD_DAT6		I	175	B3	D5	Removed
PC[9]	41	0000_0010	E2UC_7_Y		O	2	C3	D4	Removed
PC[9]	591	0000_0010	E2UC_7_Y		I	2	C3	D4	Removed
PC[9]	767	0000_0010	ULPI1_FAULT		I	2	C3	D4	Removed
PC[11]	43	0000_0010	E2UC_1_Y	E0UC_1_G	O	35	K4	M4	Changed
PC[11]	513	0000_0101		E0UC_1_G	I	35	K4	M4	Added
PC[11]	585	0000_0010	E2UC_1_Y		I	35	K4	M4	Removed

Hardware differences

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PC[12]	44	0000_0011	SD_DAT4		O	173	B4	D6	Removed
PC[12]	986	0000_0001	SD_DAT4		I	173	B4	D6	Removed
PC[13]	45	0000_0100	SD_DAT5		O	174	A3	E6	Removed
PC[13]	987	0000_0001	SD_DAT5		I	174	A3	E6	Removed
PC[14]	46	0000_0011	E2UC_6_Y		O	3	B2	B2	Removed
PC[14]	590	0000_0010	E2UC_6_Y		I	3	B2	B2	Removed
PC[15]	47	0000_0011	E2UC_5_Y		O	4	A1	C3	Removed
PC[15]	589	0000_0011	E2UC_5_Y		I	4	A1	C3	Removed
PD[9]	974	0000_0010	MII_1_RXD[1]		I	94	N16	N15	Removed
PD[10]	973	0000_0010	MII_1_RXD[0]		I	95	M14	P15	Removed
PD[12]	60	0000_0100	ENET1_TMR1		O	100	L13	N16	Removed
PD[12]	846	0000_0001	ENET1_TMR1		I	100	L13	N16	Removed
PD[14]	976	0000_0001	MII_1_RXD[3]		I	104	K13	T17	Removed
PD[15]	1020	0000_0001	MLBDAT		I	106	J13	P17	Removed
PD[15]	63	0000_0100	MLBDAT		O	106	J13	P17	Removed
PD[15]	974	0000_0001	MII_1_RXD[1]		I	106	J13	P17	Removed
PE[2]	66	0000_0011	SD_DAT3		O	156	A7	A12	Removed
PE[2]	744	0000_0001	ULPI0_CLK		I	156	A7	A12	Removed
PE[2]	985	0000_0001	SD_DAT3		I	156	A7	A12	Removed
PE[3]	67	0000_0011	SD_CMD		O	157	A10	D10	Removed
PE[3]	746	0000_0001	ULPI0_NXT		I	157	A10	D10	Removed
PE[3]	980	0000_0001	SD_CMD		I	157	A10	D10	Removed
PE[4]	68	0000_0100	SD_DAT1		O	160	A8	B11	Removed
PE[4]	68	0000_0101	ULPI0_D2		O	160	A8	B11	Removed
PE[4]	749	0000_0001	ULPI0_D2		I	160	A8	B11	Removed
PE[4]	983	0000_0001	SD_DAT1		I	160	A8	B11	Removed
PE[5]	69	0000_0100	SD_DAT2		O	161	B8	A10	Removed
PE[5]	69	0000_0101	ULPI0_D3		O	161	B8	A10	Removed
PE[5]	750	0000_0001	ULPI0_D3		I	161	B8	A10	Removed
PE[5]	984	0000_0001	SD_DAT2		I	161	B8	A10	Removed
PE[6]	70	0000_0101	SD_CMD		O	167	B6	F8	Removed
PE[6]	980	0000_0010	SD_CMD		I	167	B6	F8	Removed
PE[7]	71	0000_0101	SD_CLK		O	168	A5	D7	Removed
PE[7]	990	0000_0001	SD_CLK		I	168	A5	D7	Removed
PE[10]	1021	0000_0001		INP (GF)	I	23	G3	H1	Added
PE[12]	767	0000_0001	ULPI1_FAULT		I	133	C14	C18	Removed
PE[12]	972	0000_0001	MII_1_TX_CLK		I	133	C14	C18	Removed
PE[14]	760	0000_0001	ULPI1_D2		I	136	A14	C15	Removed

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Port	SIUL MSCR#	MSCR SSS	MPC5748G Function	MPC5746C Function	Dir	176 LQFP	256 BGA	324 BGA	difference
PE[14]	78	0000_0011	ULPI1_D2		O	136	A14	C15	Removed
PE[15]	761	0000_0001	ULPI1_D3		I	137	C12	E12	Removed
PE[15]	79	0000_0100	ULPI1_D3		O	137	C12	E12	Removed
PF[0]	80	0000_0011	SOUT_4		O	63	P7	N9	Removed
PF[1]	824	0000_0001	SIN_4		I	64	T6	R9	Removed
PF[2]	1018	0000_0101		INP (GF)	I	65	R6	P10	Added
PF[2]	82	0000_0011	SCLK_4		O	65	R6	P10	Removed
PF[2]	825	0000_0001	SCLK_4		I	65	R6	P10	Removed
PF[3]	1019	0000_0111		INP (GF)	I	66	R7	U10	Added
PF[3]	826	0000_0001	SS_4		I	66	R7	U10	Removed
PF[3]	83	0000_0011	CS0_4		O	66	R7	U10	Removed
PF[4]	1020	0000_0111		INP (GF)	I	67	R8	N10	Added
PF[4]	84	0000_0011	SOUT_5		O	67	R8	N10	Removed
PF[5]	1021	0000_1001		INP (GF)	I	68	P8	V12	Added
PF[5]	827	0000_0001	SIN_5		I	68	P8	V12	Removed
PF[6]	542	0000_0101		E0UC_30_Y	I	69	N8	T11	Added
PF[6]	614	0000_0100	E2UC_30_Y		I	69	N8	T11	Removed
PF[6]	828	0000_0001	SCLK_5		I	69	N8	T11	Removed
PF[6]	86	0000_0011	SCLK_5		O	69	N8	T11	Removed
PF[6]	86	0000_0101	E2UC_30_Y	E0UC_30_Y	O	69	N8	T11	Changed
PF[7]	829	0000_0001	SS_5		I	70	P9	R10	Removed
PF[7]	87	0000_0011	CS0_5		O	70	P9	R10	Removed
PF[8]	527	0000_0011		E0UC_15_H	I	42	N2	T2	Added
PF[8]	599	0000_0010	E2UC_15_Y		I	42	N2	T2	Removed
PF[8]	88	0000_0100	E2UC_15_Y	E0UC_15_H	O	42	N2	T2	Changed
PF[9]	526	0000_0101		E0UC_14_H	I	41	M4	T1	Added
PF[9]	598	0000_0010	E2UC_14_Y		I	41	M4	T1	Removed
PF[9]	89	0000_0011	E2UC_14_Y	E0UC_14_H	O	41	M4	T1	Changed
PF[10]	531	0000_0011		E0UC_19_Y	I	46	P2	R5	Added
PF[10]	603	0000_0010	E2UC_19_Y		I	46	P2	R5	Removed
PF[10]	90	0000_0100	E2UC_19_Y	E0UC_19_Y	O	46	P2	R5	Changed
PF[11]	532	0000_0011		E0UC_20_Y	I	47	R1	P5	Added
PF[11]	604	0000_0010	E2UC_20_Y		I	47	R1	P5	Removed
PF[11]	91	0000_0011	E2UC_20_Y	E0UC_20_Y	O	47	R1	P5	Changed
PF[12]	528	0000_0011		E0UC_16_X	I	43	P1	N5	Added
PF[12]	600	0000_0010	E2UC_16_X		I	43	P1	N5	Removed
PF[12]	92	0000_0011	E2UC_16_X	E0UC_16_X	O	43	P1	N5	Changed
PF[13]	534	0000_0101		E0UC_22_X	I	49	P3	N6	Added

Hardware differences

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PF[13]	606	0000_0011	E2UC_22_X		I	49	P3	N6	Removed
PF[13]	93	0000_0010	E2UC_22_X	E0UC_22_X	O	49	P3	N6	Changed
PG[3]	585	0000_0011	E2UC_1_Y		I	15	E1	J5	Removed
PG[3]	99	0000_0011	E2UC_1_Y		O	15	E1	J5	Removed
PG[5]	101	0000_0010	E2UC_2_Y	E0UC_2_G	O	13	D1	F2	Changed
PG[5]	514	0000_0100		E0UC_2_G	I	13	D1	F2	Added
PG[5]	586	0000_0010	E2UC_2_Y		I	13	D1	F2	Removed
PG[6]	102	0000_0100	E2UC_3_Y	E0UC_3_G	O	38	M1	M2	Changed
PG[6]	515	0000_0110		E0UC_3_G	I	38	M1	M2	Added
PG[6]	587	0000_0010	E2UC_3_Y		I	38	M1	M2	Removed
PG[7]	1021	0000_0010		INP (GF)	I	37	L2	M1	Added
PG[7]	103	0000_0100	E2UC_2_Y		O	37	L2	M1	Removed
PG[7]	586	0000_0011	E2UC_2_Y		I	37	L2	M1	Removed
PG[9]	105	0000_0011	E2UC_0_X	E0UC_0_X	O	33	J4	L3	Changed
PG[9]	512	0000_0101		E0UC_0_X	I	33	J4	L3	Added
PG[9]	584	0000_0011	E2UC_0_X		I	33	J4	L3	Removed
PG[10]	1021	0000_0110		INP (GF)	I	138	B13	D14	Added
PG[10]	106	0000_0011	ULPI1_D4		O	138	B13	D14	Removed
PG[10]	762	0000_0001	ULPI1_D4		I	138	B13	D14	Removed
PG[11]	107	0000_0100	ULPI1_D5		O	139	A16	D13	Removed
PG[11]	763	0000_0001	ULPI1_D5		I	139	A16	D13	Removed
PG[12]	108	0000_0011	E2UC_12_Y		O	116	F15	L18	Removed
PG[12]	596	0000_0010	E2UC_12_Y		I	116	F15	L18	Removed
PG[13]	109	0000_0011	E2UC_13_Y		O	115	F16	M18	Removed
PG[13]	597	0000_0010	E2UC_13_Y		I	115	F16	M18	Removed
PG[14]	110	0000_0011	ULPI1_D0		O	134	C13	F12	Removed
PG[14]	758	0000_0001	ULPI1_D0		I	134	C13	F12	Removed
PG[15]	111	0000_0011	ULPI1_D1		O	135	D13	C16	Removed
PG[15]	759	0000_0001	ULPI1_D1		I	135	D13	C16	Removed
PH[0]	112	0000_0010	E2UC_11_Y		O	117	E15	L17	Removed
PH[0]	595	0000_0010	E2UC_11_Y		I	117	E15	L17	Removed
PH[1]	113	0000_0011	E2UC_10_Y		O	118	F13	K18	Removed
PH[1]	594	0000_0010	E2UC_10_Y		I	118	F13	K18	Removed
PH[2]	114	0000_0011	E2UC_9_Y		O	119	D16	J18	Removed
PH[2]	593	0000_0010	E2UC_9_Y		I	119	D16	J18	Removed
PH[3]	115	0000_0100	MII_1_TXD[2]		O	120	F14	J17	Removed
PH[4]	116	0000_0100	ULPI0_D4		O	162	D7	C10	Removed
PH[4]	751	0000_0001	ULPI0_D4		I	162	D7	C10	Removed

Migrating between MPC5748G and MPC5746C, Rev. 0, June 2015

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PH[5]	117	0000_0011	ULPI0_D5		O	163	B7	B10	Removed
PH[5]	752	0000_0001	ULPI0_D5		I	163	B7	B10	Removed
PH[6]	118	0000_0101	ULPI0_D6		O	164	C7	A9	Removed
PH[6]	753	0000_0001	ULPI0_D6		I	164	C7	A9	Removed
PH[7]	119	0000_0110	ULPI0_D7		O	165	C6	D9	Removed
PH[7]	754	0000_0001	ULPI0_D7		I	165	C6	D9	Removed
PH[8]	120	0000_0101	SD_RST		O	166	A6	E8	Removed
PH[8]	981	0000_0001	SD_WP		I	166	A6	E8	Removed
PH[11]	123	0000_0100	ULPI1_D6		O	140	A13	C14	Removed
PH[11]	764	0000_0001	ULPI1_D6		I	140	A13	C14	Removed
PH[12]	124	0000_0100	ULPI1_D7		O	141	B12	D12	Removed
PH[12]	765	0000_0001	ULPI1_D7		I	141	B12	D12	Removed
PH[15]	127	0000_0010	E2UC_3_Y		O	8	E3	G4	Removed
PH[15]	587	0000_0011	E2UC_3_Y		I	8	E3	G4	Removed
PI[0]	1018	0000_0010		INP (GF)	I	172	C5	C6	Added
PI[0]	128	0000_0100	SD_DAT3		O	172	C5	C6	Removed
PI[0]	985	0000_0010	SD_DAT3		I	172	C5	C6	Removed
PI[1]	1018	0000_0100		INP (GF)	I	171	A4	E7	Added
PI[1]	129	0000_0011	SD_DAT2		O	171	A4	E7	Removed
PI[1]	984	0000_0010	SD_DAT2		I	171	A4	E7	Removed
PI[2]	1019	0000_0011		INP (GF)	I	170	D6	C7	Added
PI[2]	130	0000_0100	SD_DAT1		O	170	D6	C7	Removed
PI[2]	983	0000_0010	SD_DAT1		I	170	D6	C7	Removed
PI[3]	1019	0000_0110		INP (GF)	I	169	B5	C8	Added
PI[3]	131	0000_0011	SD_DAT0		O	169	B5	C8	Removed
PI[3]	982	0000_0010	SD_DAT0		I	169	B5	C8	Removed
PI[4]	1020	0000_0010		INP (GF)	I	143	A12	A18	Added
PI[4]	132	0000_0011	ULPI1_STP		O	143	A12	A18	Removed
PI[5]	1020	0000_0101		INP (GF)	I	142	D12	E11	Added
PI[5]	757	0000_0001	ULPI1_NXT		I	142	D12	E11	Removed
PI[6]	1021	0000_0011		INP (GF)	I	11	D2	H4	Added
PI[7]	1021	0000_0111		INP (GF)	I	12	E2	G3	Added
PI[8]	1018	0000_0001	MLBCLK		I	108	J14	P18	Removed
PI[8]	136	0000_0001	E2UC_15_Y		O	108	J14	P18	Removed
PI[8]	599	0000_0011	E2UC_15_Y		I	108	J14	P18	Removed
PI[8]	971	0000_0001	MII_1_RX_CLK		I	108	J14	P18	Removed
PI[9]	137	0000_0001	E2UC_20_Y		O	-	J15	T12	Removed
PI[9]	604	0000_0011	E2UC_20_Y		I	-	J15	T12	Removed

Hardware differences

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PI[10]	138	0000_0001	E2UC_21_Y		O	-	J16	U12	Removed
PI[10]	605	0000_0011	E2UC_21_Y		I	-	J16	U12	Removed
PI[11]	139	0000_0001	E2UC_14_Y		O	111	H16	N18	Removed
PI[11]	598	0000_0011	E2UC_14_Y		I	111	H16	N18	Removed
PI[12]	140	0000_0011	MII_1_TX_EN		O	112	G15	N17	Removed
PI[13]	141	0000_0011	MII_1_TXD[3]		O	113	G14	M16	Removed
PJ[0]	144	0000_0100	E2UC_19_Y		O	74	R11	U18	Removed
PJ[0]	602	0000_0101	E2UC_19_Y		I	74	R11	U18	Removed
PJ[4]	148	0000_0011	E2UC_4_Y		O	5	D3	A1	Removed
PJ[4]	588	0000_0011	E2UC_4_Y		I	5	D3	A1	Removed
PJ[5]	149	0000_0001	E2UC_16_X		O	-	N12	T16	Removed
PJ[5]	600	0000_0011	E2UC_16_X		I	-	N12	T16	Removed
PJ[6]	150	0000_0001	E2UC_17_Y		O	-	N15	U16	Removed
PJ[6]	601	0000_0011	E2UC_17_Y		I	-	N15	U16	Removed
PJ[7]	151	0000_0001	E2UC_18_Y		O	-	P16	U17	Removed
PJ[7]	602	0000_0011	E2UC_18_Y		I	-	P16	U17	Removed
PJ[8]	152	0000_0001	E2UC_19_Y		O	-	P15	U13	Removed
PJ[8]	603	0000_0011	E2UC_19_Y		I	-	P15	U13	Removed
PJ[13]	157	0000_0010	CS0_5		O	-	N5	T6	Removed
PJ[13]	829	0000_0010	SS_5		I	-	N5	T6	Removed
PJ[14]	158	0000_0101	SCLK_5		O	-	T4	R6	Removed
PJ[14]	828	0000_0010	SCLK_5		I	-	T4	R6	Removed
PJ[15]	159	0000_0011	SOUT_5		O	-	R4	U4	Removed
PK[0]	827	0000_0010	SIN_5		I	-	T3	T4	Removed
PK[1]	161	0000_0010	E2UC_6_Y	E0UC_6_G	O	-	H4	N3	Changed
PK[1]	518	0000_0100		E0UC_6_G	I	-	H4	N3	Added
PK[1]	590	0000_0011	E2UC_6_Y		I	-	H4	N3	Removed
PK[2]	162	0000_0010	E2UC_7_Y		O	-	L4	N4	Removed
PK[2]	591	0000_0011	E2UC_7_Y		I	-	L4	N4	Removed
PK[3]	163	0000_0010	E2UC_8_X		O	-	N1	P1	Removed
PK[3]	592	0000_0011	E2UC_8_X		I	-	N1	P1	Removed
PK[4]	164	0000_0100	E2UC_9_Y	E0UC_9_H	O	-	M3	P2	Changed
PK[4]	521	0000_0011		E0UC_9_H	I	-	M3	P2	Added
PK[4]	593	0000_0011	E2UC_9_Y		I	-	M3	P2	Removed
PK[5]	165	0000_0001	E2UC_10_Y	E0UC_10_H	O	-	M5	P3	Changed
PK[5]	522	0000_0100		E0UC_10_H	I	-	M5	P3	Added
PK[5]	594	0000_0011	E2UC_10_Y		I	-	M5	P3	Removed
PK[6]	166	0000_0011	E2UC_11_Y	E0UC_11_H	O	-	M6	P4	Changed

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PK[6]	523	0000_0100		E0UC_11_H	I	-	M6	P4	Added
PK[6]	595	0000_0011	E2UC_11_Y		I	-	M6	P4	Removed
PK[7]	167	0000_0001	E2UC_12_Y	E0UC_12_H	O	-	M7	R1	Changed
PK[7]	524	0000_0100		E0UC_12_H	I	-	M7	R1	Added
PK[7]	596	0000_0011	E2UC_12_Y		I	-	M7	R1	Removed
PK[8]	168	0000_0011	E2UC_13_Y	E0UC_13_H	O	-	M8	R2	Changed
PK[8]	525	0000_0101		E0UC_13_H	I	-	M8	R2	Added
PK[8]	597	0000_0011	E2UC_13_Y		I	-	M8	R2	Removed
PK[9]	1020	0000_0110		INP (GF)	I	-	E8	B7	Added
PK[10]	1021	0000_0100		INP (GF)	I	-	E7	A6	Added
PK[11]	1021	0000_1000		INP (GF)	I	-	F8	B6	Added
PL[2]	178	0000_0010	ULPI1_D6		O	-	-	E15	Removed
PL[2]	178	0000_0011	dCS1_1		O	-	-	E15	Removed
PL[2]	764	0000_0010	ULPI1_D6		I	-	-	E15	Removed
PL[3]	179	0000_0010	ULPI1_D5		O	-	-	E14	Removed
PL[3]	179	0000_0011	dCS2_1		O	-	-	E14	Removed
PL[3]	763	0000_0010	ULPI1_D5		I	-	-	E14	Removed
PL[4]	180	0000_0010	ULPI1_D4		O	-	-	F13	Removed
PL[4]	180	0000_0011	dCS3_1		O	-	-	F13	Removed
PL[4]	762	0000_0010	ULPI1_D4		I	-	-	F13	Removed
PL[5]	181	0000_0010	ULPI1_D3		O	-	-	F14	Removed
PL[5]	181	0000_0011	dCS4_1		O	-	-	F14	Removed
PL[5]	761	0000_0010	ULPI1_D3		I	-	-	F14	Removed
PL[6]	182	0000_0010	ULPI1_D2		O	-	-	F15	Removed
PL[6]	760	0000_0010	ULPI1_D2		I	-	-	F15	Removed
PL[7]	183	0000_0010	ULPI1_D1		O	-	-	G13	Removed
PL[7]	183	0000_0011	E2UC_23_X		O	-	-	G13	Removed
PL[7]	607	0000_0100	E2UC_23_X		I	-	-	G13	Removed
PL[7]	759	0000_0010	ULPI1_D1		I	-	-	G13	Removed
PL[8]	755	0000_0010	ULPI1_CLK		I	-	-	D15	Removed
PL[9]	185	0000_0010	ULPI1_STP		O	-	-	E13	Removed
PL[9]	185	0000_0011	dSOUT_1		O	-	-	E13	Removed
PL[10]	186	0000_0010	ULPI1_D7		O	-	-	G12	Removed
PL[10]	186	0000_0011	dCS0_1		O	-	-	G12	Removed
PL[10]	765	0000_0010	ULPI1_D7		I	-	-	G12	Removed
PL[10]	805	0000_0110	dSS_1		I	-	-	G12	Removed
PL[11]	757	0000_0010	ULPI1_NXT		I	-	-	E16	Removed
PL[11]	803	0000_0101	dSIN_1		I	-	-	E16	Removed

Hardware differences

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PL[12]	188	0000_0010	dSCLK_1		O	-	-	D16	Removed
PL[12]	756	0000_0010	ULPI1_DIR		I	-	-	D16	Removed
PL[12]	804	0000_0100	dSCLK_1		I	-	-	D16	Removed
PL[13]	189	0000_0010	ULPI1_D0		O	-	-	F16	Removed
PL[13]	189	0000_0011	E2UC_22_X		O	-	-	F16	Removed
PL[13]	606	0000_0100	E2UC_22_X		I	-	-	F16	Removed
PL[13]	758	0000_0010	ULPI1_D0		I	-	-	F16	Removed
PL[14]	1003	0000_0011	SAIO_D0		I	-	-	G16	Removed
PL[14]	190	0000_0010	SAIO_D0		O	-	-	G16	Removed
PL[14]	190	0000_0011	E0UC_13_H		O	-	-	G16	Removed
PL[14]	525	0000_0101	E0UC_13_H		I	-	-	G16	Removed
PL[15]	1004	0000_0010	SAIO_D1		I	-	-	G15	Removed
PL[15]	191	0000_0010	SAIO_D1		O	-	-	G15	Removed
PL[15]	191	0000_0011	E0UC_0_X		O	-	-	G15	Removed
PL[15]	512	0000_0101	E0UC_0_X		I	-	-	G15	Removed
PM[0]	1005	0000_0010	SAIO_D2		I	-	-	G14	Removed
PM[0]	192	0000_0010	SAIO_D2		O	-	-	G14	Removed
PM[1]	1006	0000_0010	SAIO_D3		I	-	-	H13	Removed
PM[1]	193	0000_0010	SAIO_D3		O	-	-	H13	Removed
PM[2]	1000	0000_0010	SAIO_BCLK		I	-	-	H15	Removed
PM[2]	194	0000_0010	SAIO_BCLK		O	-	-	H15	Removed
PM[4]	196	0000_0010	ENET1_TMR2		O	-	L12	K15	Removed
PM[4]	847	0000_0001	ENET1_TMR2		I	-	L12	K15	Removed
PM[6]	1000	0000_0011	SAIO_BCLK		I	-	-	L16	Removed
PM[6]	198	0000_0001	SAIO_BCLK		O	-	-	L16	Removed
PM[7]	1002	0000_0010	SAIO_SYNC		I	-	-	H16	Removed
PM[7]	199	0000_0010	SAIO_SYNC		O	-	-	H16	Removed
PM[8]	1001	0000_0010	SAIO_MCLK		I	-	-	J13	Removed
PM[8]	200	0000_0010	SAIO_MCLK		O	-	-	J13	Removed
PM[8]	200	0000_0011	ADC0_MA[2]		O	-	-	J13	Removed
PM[9]	201	0000_0010	ADC0_MA[1]		O	-	-	H14	Removed
PM[10]	202	0000_0010	ADC0_MA[0]		O	-	-	J14	Removed
PM[11]	203	0000_0000	GPIO[203]		I/O	-	-	G10	Removed
PM[11]	680	0000_0001	EIRQ24		I	-	-	G10	Removed
PM[11]	706	0000_0011	CAN6RX		I	-	-	G10	Removed
PM[11]	724	0000_0001	LIN12RX		I	-	-	G10	Removed
PM[12]	204	0000_0000	GPIO[204]		I/O	-	-	G11	Removed
PM[12]	204	0000_0001	LIN12TX		O	-	-	G11	Removed

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PM[12]	204	0000_0010	CAN6TX		O	-	-	G11	Removed
PM[13]	1002	0000_0011	SAIO_SYNC		I	-	-	M13	Removed
PM[13]	205	0000_0001	SAIO_SYNC		O	-	-	M13	Removed
PM[13]	205	-	ADC1_S[14]		O	-	-	M13	Removed
PM[15]	207	0000_0000	GPIO[207]		I/O	-	-	T10	Removed
PM[15]	207	0000_0001	E2UC_22_X		O	-	-	T10	Removed
PM[15]	207	-	ADC0_S[32]		O	-	-	T10	Removed
PM[15]	606	0000_0101	E2UC_22_X		I	-	-	T10	Removed
PN[0]	208	0000_0000	GPIO[208]		I/O	-	-	T9	Removed
PN[0]	208	0000_0001	E2UC_23_X		O	-	-	T9	Removed
PN[0]	208	-	ADC0_S[33]		O	-	-	T9	Removed
PN[0]	607	0000_0101	E2UC_23_X		I	-	-	T9	Removed
PN[1]	209	0000_0000	GPIO[209]		I/O	-	-	V11	Removed
PN[1]	209	0000_0001	E2UC_24_X		O	-	-	V11	Removed
PN[1]	209	-	ADC0_S[34]		O	-	-	V11	Removed
PN[1]	608	0000_0100	E2UC_24_X		I	-	-	V11	Removed
PN[2]	210	0000_0000	GPIO[210]		I/O	-	-	U9	Removed
PN[2]	210	0000_0001	E2UC_25_Y		O	-	-	U9	Removed
PN[2]	210	-	ADC0_S[35]		O	-	-	U9	Removed
PN[2]	609	0000_0011	E2UC_25_Y		I	-	-	U9	Removed
PN[3]	211	0000_0000	GPIO[211]		I/O	-	-	T8	Removed
PN[3]	211	0000_0001	E2UC_26_Y		O	-	-	T8	Removed
PN[3]	211	-	ADC0_S[36]		O	-	-	T8	Removed
PN[3]	610	0000_0011	E2UC_26_Y		I	-	-	T8	Removed
PN[4]	212	0000_0000	GPIO[212]		I/O	-	-	U7	Removed
PN[4]	212	0000_0001	E2UC_27_Y		O	-	-	U7	Removed
PN[4]	212	-	ADC0_S[37]		O	-	-	U7	Removed
PN[4]	611	0000_0010	E2UC_27_Y		I	-	-	U7	Removed
PN[5]	213	0000_0000	GPIO[213]		I/O	-	-	R8	Removed
PN[5]	213	0000_0001	E2UC_28_Y		O	-	-	R8	Removed
PN[5]	213	-	ADC0_S[38]		O	-	-	R8	Removed
PN[5]	612	0000_0010	E2UC_28_Y		I	-	-	R8	Removed
PN[6]	214	0000_0000	GPIO[214]		I/O	-	-	P8	Removed
PN[6]	214	0000_0001	E2UC_29_Y		O	-	-	P8	Removed
PN[6]	214	-	ADC0_S[39]		O	-	-	P8	Removed
PN[6]	613	0000_0010	E2UC_29_Y		I	-	-	P8	Removed
PN[7]	215	0000_0000	GPIO[215]		I/O	-	-	U6	Removed
PN[7]	215	0000_0001	E2UC_30_Y		O	-	-	U6	Removed

Hardware differences

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PN[7]	215	-	ADCO_S[40]		O	-	-	U6	Removed
PN[7]	614	0000_0010	E2UC_30_Y		I	-	-	U6	Removed
PN[8]	216	0000_0000	GPIO[216]		I/O	-	-	U5	Removed
PN[8]	216	0000_0001	E2UC_31_Y		O	-	-	U5	Removed
PN[8]	216	0000_0010	E1UC_20_Y		O	-	-	U5	Removed
PN[8]	216	0000_0011	E2UC_29_Y		O	-	-	U5	Removed
PN[8]	216	-	ADCO_S[41]		O	-	-	U5	Removed
PN[8]	568	0000_0011	E1UC_20_Y		I	-	-	U5	Removed
PN[8]	613	0000_0011	E2UC_29_Y		I	-	-	U5	Removed
PN[8]	615	0000_0010	E2UC_31_Y		I	-	-	U5	Removed
PN[8]	705	0000_0100	CAN5RX		I	-	-	U5	Removed
PN[9]	217	0000_0000	GPIO[217]		I/O	-	-	T5	Removed
PN[9]	217	0000_0010	E1UC_19_Y		O	-	-	T5	Removed
PN[9]	217	0000_0011	CAN5TX		O	-	-	T5	Removed
PN[9]	217	0000_0100	E2UC_28_Y		O	-	-	T5	Removed
PN[9]	217	-	ADCO_S[42]		O	-	-	T5	Removed
PN[9]	567	0000_0011	E1UC_19_Y		I	-	-	T5	Removed
PN[9]	612	0000_0011	E2UC_28_Y		I	-	-	T5	Removed
PN[10]	218	0000_0000	GPIO[218]		I/O	-	-	T7	Removed
PN[10]	218	0000_0010	E1UC_18_Y		O	-	-	T7	Removed
PN[10]	218	0000_0011	E2UC_27_Y		O	-	-	T7	Removed
PN[10]	218	-	ADCO_S[43]		O	-	-	T7	Removed
PN[10]	566	0000_0100	E1UC_18_Y		I	-	-	T7	Removed
PN[10]	611	0000_0011	E2UC_27_Y		I	-	-	T7	Removed
PN[11]	219	0000_0000	GPIO[219]		I/O	-	-	V2	Removed
PN[11]	219	0000_0001	CAN1TX		O	-	-	V2	Removed
PN[11]	219	0000_0010	E1UC_9_H		O	-	-	V2	Removed
PN[11]	557	0000_0011	E1UC_9_H		I	-	-	V2	Removed
PN[12]	220	0000_0000	GPIO[220]		I/O	-	-	V1	Removed
PN[12]	220	0000_0001	E1UC_8_X		O	-	-	V1	Removed
PN[12]	556	0000_0011	E1UC_8_X		I	-	-	V1	Removed
PN[12]	701	0000_0111	CAN1RX		I	-	-	V1	Removed
PN[13]	221	0000_0000	GPIO[221]		I/O	-	-	U1	Removed
PN[13]	221	0000_0001	CAN0TX		O	-	-	U1	Removed
PN[13]	221	0000_0010	E0UC_30_Y		O	-	-	U1	Removed
PN[13]	542	0000_0101	E0UC_30_Y		I	-	-	U1	Removed
PN[14]	222	0000_0000	GPIO[222]		I/O	-	-	R4	Removed
PN[14]	222	0000_0001	E0UC_31_Y		O	-	-	R4	Removed

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PN[14]	543	0000_0101	E0UC_31_Y		I	-	-	R4	Removed
PN[14]	700	0000_0011	CAN0RX		I	-	-	R4	Removed
PN[15]	223	0000_0000	GPIO[223]		I/O	-	-	L4	Removed
PN[15]	223	0000_0001	E2UC_21_Y		O	-	-	L4	Removed
PN[15]	605	0000_0100	E2UC_21_Y		I	-	-	L4	Removed
PO[0]	224	0000_0001	E2UC_20_Y		O	-	K5	G1	Removed
PO[0]	604	0000_0100	E2UC_20_Y		I	-	K5	G1	Removed
PO[1]	225	0000_0001	E2UC_19_Y		O	-	L5	F1	Removed
PO[1]	603	0000_0100	E2UC_19_Y		I	-	L5	F1	Removed
PO[2]	226	0000_0000	GPIO[226]		I/O	-	-	M6	Removed
PO[2]	226	0000_0001	LIN13TX		O	-	-	M6	Removed
PO[2]	226	0000_0010	E2UC_18_Y		O	-	-	M6	Removed
PO[2]	602	0000_0100	E2UC_18_Y		I	-	-	M6	Removed
PO[3]	227	0000_0000	GPIO[227]		I/O	-	-	L6	Removed
PO[3]	227	0000_0001	E2UC_17_Y		O	-	-	L6	Removed
PO[3]	601	0000_0100	E2UC_17_Y		I	-	-	L6	Removed
PO[3]	686	0000_0001	EIRQ30		I	-	-	L6	Removed
PO[3]	725	0000_0001	LIN13RX		I	-	-	L6	Removed
PO[4]	228	0000_0000	GPIO[228]		I/O	-	-	E1	Removed
PO[4]	228	0000_0001	E1UC_0_X		O	-	-	E1	Removed
PO[4]	548	0000_0100	E1UC_0_X		I	-	-	E1	Removed
PO[5]	229	0000_0000	GPIO[229]		I/O	-	-	H6	Removed
PO[5]	229	0000_0001	LIN14TX		O	-	-	H6	Removed
PO[5]	229	0000_0010	E2UC_16_X		O	-	-	H6	Removed
PO[5]	600	0000_0100	E2UC_16_X		I	-	-	H6	Removed
PO[6]	230	0000_0000	GPIO[230]		I/O	-	-	H5	Removed
PO[6]	230	0000_0001	E2UC_15_Y		O	-	-	H5	Removed
PO[6]	599	0000_0100	E2UC_15_Y		I	-	-	H5	Removed
PO[6]	685	0000_0001	EIRQ29		I	-	-	H5	Removed
PO[6]	726	0000_0001	LIN14RX		I	-	-	H5	Removed
PO[7]	231	0000_0000	GPIO[231]		I/O	-	-	D1	Removed
PO[7]	231	0000_0001	LIN15TX		O	-	-	D1	Removed
PO[7]	231	0000_0010	E2UC_14_Y		O	-	-	D1	Removed
PO[7]	598	0000_0100	E2UC_14_Y		I	-	-	D1	Removed
PO[8]	232	0000_0000	GPIO[232]		I/O	-	-	D2	Removed
PO[8]	232	0000_0001	E2UC_13_Y		O	-	-	D2	Removed
PO[8]	597	0000_0100	E2UC_13_Y		I	-	-	D2	Removed
PO[8]	684	0000_0001	EIRQ28		I	-	-	D2	Removed

Hardware differences

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PO[8]	727	0000_0001	LIN15RX		I	-	-	D2	Removed
PO[9]	233	0000_0000	GPIO[233]		I/O	-	-	E3	Removed
PO[9]	233	0000_0001	LIN16TX		O	-	-	E3	Removed
PO[9]	233	0000_0010	E2UC_12_Y		O	-	-	E3	Removed
PO[9]	596	0000_0100	E2UC_12_Y		I	-	-	E3	Removed
PO[10]	234	0000_0000	GPIO[234]		I/O	-	-	D3	Removed
PO[10]	234	0000_0001	E2UC_11_Y		O	-	-	D3	Removed
PO[10]	595	0000_0100	E2UC_11_Y		I	-	-	D3	Removed
PO[10]	683	0000_0001	EIRQ27		I	-	-	D3	Removed
PO[10]	728	0000_0001	LIN16RX		I	-	-	D3	Removed
PO[11]	235	0000_0000	GPIO[235]		I/O	-	-	C1	Removed
PO[11]	235	0000_0001	LIN17TX		O	-	-	C1	Removed
PO[11]	235	0000_0010	E2UC_10_Y		O	-	-	C1	Removed
PO[11]	594	0000_0100	E2UC_10_Y		I	-	-	C1	Removed
PO[12]	236	0000_0000	GPIO[236]		I/O	-	-	B1	Removed
PO[12]	236	0000_0001	E2UC_9_Y		O	-	-	B1	Removed
PO[12]	593	0000_0100	E2UC_9_Y		I	-	-	B1	Removed
PO[12]	682	0000_0001	EIRQ26		I	-	-	B1	Removed
PO[12]	729	0000_0001	LIN17RX		I	-	-	B1	Removed
PO[13]	237	0000_0000	GPIO[237]		I/O	-	-	E4	Removed
PO[13]	237	0000_0001	CAN6TX		O	-	-	E4	Removed
PO[13]	237	0000_0010	E2UC_8_X		O	-	-	E4	Removed
PO[13]	592	0000_0100	E2UC_8_X		I	-	-	E4	Removed
PO[14]	238	0000_0000	GPIO[238]		I/O	-	-	F4	Removed
PO[14]	238	0000_0001	E2UC_7_Y		O	-	-	F4	Removed
PO[14]	591	0000_0100	E2UC_7_Y		I	-	-	F4	Removed
PO[14]	681	0000_0001	EIRQ25		I	-	-	F4	Removed
PO[14]	706	0000_0100	CAN6RX		I	-	-	F4	Removed
PO[15]	239	0000_0000	GPIO[239]		I/O	-	-	G6	Removed
PO[15]	239	0000_0001	CAN7TX		O	-	-	G6	Removed
PO[15]	239	0000_0010	E2UC_6_Y		O	-	-	G6	Removed
PO[15]	590	0000_0100	E2UC_6_Y		I	-	-	G6	Removed
PP[0]	240	0000_0000	GPIO[240]		I/O	-	-	G5	Removed
PP[0]	240	0000_0001	E2UC_5_Y		O	-	-	G5	Removed
PP[0]	589	0000_0100	E2UC_5_Y		I	-	-	G5	Removed
PP[0]	707	0000_0011	CAN7RX		I	-	-	G5	Removed
PP[1]	241	0000_0000	GPIO[241]		I/O	-	-	B3	Removed
PP[1]	241	0000_0001	E2UC_4_Y		O	-	-	B3	Removed

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PP[1]	588	0000_0100	E2UC_4_Y		I	-	-	B3	Removed
PP[1]	827	0000_0011	SIN_5		I	-	-	B3	Removed
PP[2]	242	0000_0000	GPIO[242]		I/O	-	-	C4	Removed
PP[2]	242	0000_0001	CS0_5		O	-	-	C4	Removed
PP[2]	242	0000_0010	E2UC_3_Y		O	-	-	C4	Removed
PP[2]	587	0000_0100	E2UC_3_Y		I	-	-	C4	Removed
PP[2]	829	0000_0011	SS_5		I	-	-	C4	Removed
PP[3]	243	0000_0000	GPIO[243]		I/O	-	-	F7	Removed
PP[3]	243	0000_0001	SCLK_5		O	-	-	F7	Removed
PP[3]	243	0000_0010	E2UC_2_Y		O	-	-	F7	Removed
PP[3]	586	0000_0100	E2UC_2_Y		I	-	-	F7	Removed
PP[3]	828	0000_0011	SCLK_5		I	-	-	F7	Removed
PP[4]	244	0000_0000	GPIO[244]		I/O	-	-	E5	Removed
PP[4]	244	0000_0001	SOUT_5		O	-	-	E5	Removed
PP[4]	244	0000_0010	E2UC_1_Y		O	-	-	E5	Removed
PP[4]	585	0000_0100	E2UC_1_Y		I	-	-	E5	Removed
PP[5]	245	0000_0000	GPIO[245]		I/O	-	-	G7	Removed
PP[5]	245	0000_0001	LIN0TX		O	-	-	G7	Removed
PP[5]	245	0000_0010	E2UC_0_X		O	-	-	G7	Removed
PP[5]	584	0000_0100	E2UC_0_X		I	-	-	G7	Removed
PP[6]	246	0000_0000	GPIO[246]		I/O	-	-	A2	Removed
PP[6]	246	0000_0001	SOUT_1		O	-	-	A2	Removed
PP[6]	246	0000_0010	E2UC_31_Y		O	-	-	A2	Removed
PP[6]	615	0000_0011	E2UC_31_Y		I	-	-	A2	Removed
PP[7]	247	0000_0000	GPIO[247]		I/O	-	-	A3	Removed
PP[7]	247	0000_0001	E2UC_30_Y		O	-	-	A3	Removed
PP[7]	614	0000_0011	E2UC_30_Y		I	-	-	A3	Removed
PP[7]	815	0000_0011	SIN_1		I	-	-	A3	Removed
PP[8]	248	0000_0000	GPIO[248]		I/O	-	-	B8	Removed
PP[8]	248	0000_0001	SOUT_4		O	-	-	B8	Removed
PP[8]	248	0000_0010	E2UC_29_Y		O	-	-	B8	Removed
PP[8]	613	0000_0100	E2UC_29_Y		I	-	-	B8	Removed
PP[9]	249	0000_0000	GPIO[249]		I/O	-	-	A7	Removed
PP[9]	249	0000_0001	SCLK_4		O	-	-	A7	Removed
PP[9]	249	0000_0010	E2UC_28_Y		O	-	-	A7	Removed
PP[9]	612	0000_0100	E2UC_28_Y		I	-	-	A7	Removed
PP[9]	825	0000_0010	SCLK_4		I	-	-	A7	Removed
PP[10]	250	0000_0000	GPIO[250]		I/O	-	-	A8	Removed

Hardware differences

<i>Port</i>	<i>SIUL MSCR#</i>	<i>MSCR SSS</i>	<i>MPC5748G Function</i>	<i>MPC5746C Function</i>	<i>Dir</i>	<i>176 LQFP</i>	<i>256 BGA</i>	<i>324 BGA</i>	<i>difference</i>
PP[10]	250	0000_0001	E2UC_27_Y		O	-	-	A8	Removed
PP[10]	611	0000_0100	E2UC_27_Y		I	-	-	A8	Removed
PP[10]	824	0000_0010	SIN_4		I	-	-	A8	Removed
PP[11]	251	0000_0000	GPIO[251]		I/O	-	-	B9	Removed
PP[11]	251	0000_0001	CS0_4		O	-	-	B9	Removed
PP[11]	251	0000_0010	E2UC_26_Y		O	-	-	B9	Removed
PP[11]	610	0000_0100	E2UC_26_Y		I	-	-	B9	Removed
PP[11]	826	0000_0010	SS_4		I	-	-	B9	Removed
PP[12]	252	0000_0100	ULPI0_D3		O	-	E12	B17	Removed
PP[12]	252	0000_0101	LIN16TX		O	-	E12	B17	Removed
PP[12]	750	0000_0010	ULPI0_D3		I	-	E12	B17	Removed
PP[13]	253	0000_0011	ULPI0_D2		O	-	F12	B16	Removed
PP[13]	729	0000_0010	LIN17RX		I	-	F12	B16	Removed
PP[13]	749	0000_0010	ULPI0_D2		I	-	F12	B16	Removed
PP[14]	254	0000_0011	ULPI0_D1		O	-	E11	C17	Removed
PP[14]	254	0000_0100	LIN17TX		O	-	E11	C17	Removed
PP[14]	748	0000_0010	ULPI0_D1		I	-	E11	C17	Removed
PP[15]	255	0000_0010	ULPI0_D0		O	-	F11	B18	Removed
PP[15]	747	0000_0010	ULPI0_D0		I	-	F11	B18	Removed
PQ[0]	256	0000_0010	E2UC_25_Y		O	-	J5	C11	Removed
PQ[0]	256	0000_0011	ULPI0_STP		O	-	J5	C11	Removed
PQ[0]	609	0000_0100	E2UC_25_Y		I	-	J5	C11	Removed
PQ[1]	257	0000_0010	E2UC_24_X		O	-	H5	B13	Removed
PQ[1]	608	0000_0101	E2UC_24_X		I	-	H5	B13	Removed
PQ[1]	744	0000_0010	ULPI0_CLK		I	-	H5	B13	Removed
PQ[2]	258	0000_0010	E2UC_23_X		O	-	G5	B14	Removed
PQ[2]	607	0000_0110	E2UC_23_X		I	-	G5	B14	Removed
PQ[2]	745	0000_0010	ULPI0_DIR		I	-	G5	B14	Removed
PQ[3]	259	0000_0001	E2UC_22_X		O	-	F5	F11	Removed
PQ[3]	606	0000_0110	E2UC_22_X		I	-	F5	F11	Removed
PQ[3]	746	0000_0010	ULPI0_NXT		I	-	F5	F11	Removed
PQ[4]	1020	0000_0011		INP (GF)	I	-	F6	A15	Added
PQ[4]	260	0000_0011	ULPI0_D7		O	-	F6	A15	Removed
PQ[4]	754	0000_0010	ULPI0_D7		I	-	F6	A15	Removed
PQ[5]	261	0000_0100	ULPI0_D6		O	-	E9	A16	Removed
PQ[5]	753	0000_0010	ULPI0_D6		I	-	E9	A16	Removed
PQ[6]	262	0000_0100	ULPI0_D5		O	-	F10	B15	Removed
PQ[6]	752	0000_0010	ULPI0_D5		I	-	F10	B15	Removed

Port	SIUL MSCR#	MSCR SSS	MPC5748G Function	MPC5746C Function	Dir	176 LQFP	256 BGA	324 BGA	difference
PQ[7]	263	0000_0100	ULPI0_D4		O	-	E10	A17	Removed
PQ[7]	728	0000_0010	LIN16RX		I	-	E10	A17	Removed
PQ[7]	751	0000_0010	ULPI0_D4		I	-	E10	A17	Removed

3.2. Power supply and miscellaneous pins

Besides the GPIO pinout differences, there were a few modifications to the power supply pins to add more features to the MPC5746C device. In particular, a Core Logic ground pin (VSS_LV) was removed and the internal ballast option was added.

Table 3. Power supply and miscellaneous pin differences

MPC5748G Function	MPC5746C Function	176 LQFP	256 BGA	324 BGA	Difference
VSS_LV	INT_BAL_SELECT	109	-	-	Changed
VSS_LV	INT_BAL_SELECT	-	L6	-	Changed
PM[12]	INT_BAL_SELECT	-	-	G11	Changed

Both the MPC5748G and MPC5746C devices require 1.25 V for the core logic to operate correctly. Since these devices operate at 3.3 V or 5 V supplies, there is a need to somehow generate the core logic voltage. The possible options are:

- **Internal regulation with external ballast:** In this mode, the user must place an external NPN pass transistor that is controlled by a lineal ballast controller on the MCU.
- **External regulation with bypassed ballast:** In this mode the ballast controller is bypassed and the user must provide the 1.25 V for the core logic externally. The pass transistor is not needed.

The MPC5746C provides a third option to generate these 1.25 V:

- **Internal regulation with internal ballast:** The MPC5746C device comes with an integrated PMOS FET that can be used to internally generate the 1.25 V for the core logic. In this case there is no need for the external NPN transistor. This mode is limited due to the power dissipation characteristics of the internal FET. This mode can only be used on applications where maximum current consumption (RUN_IDD) is below 160 mA.

The INT_BAL_SELECT pin is used to specify whether the Full Power Regulator (FPRG) should use the internal or an external ballast transistor. Driving the pin high will select the internal ballast transistor, driving the pin low will select an external ballast transistor. On MPC5748G boards, the INT_BAL_SELECT pin would have been a VSS_LV (ground) pin, therefore selecting external ballast usage which is the default for MPC5748G devices as they don't have the internal ballast option.

4. Booting differences

The booting mechanism is exactly the same for both the MPC5748G and MPC5746C devices, the only consideration is that they have different core configurations (the MPC5746C does not have a second e200Z4 core) and the boot headers are slightly different.

4.1. BAF

The BAF is the Boot Assist Flash module and is the one in charge of booting the MCU with the pre-defined core to its pre-defined reset vector. While the Boot header has the same general boot structure, the space were the reset vector for the second e200Z4 core was is reserved on the MPC5746C device.

Table 4. **Boot Header Structure for both devices**

<i>Address Offset</i>	<i>MPC5748G Contents</i>	<i>MPC5746C Contents</i>
0x00	Boot Header Configuration	
0x04	CPU2 Reset Vector	
0x08	Configuration Bits	
0x0C	Configuration Bits	
0x10	CPU0 Reset Vector	
0x14	CPU1 Reset Vector	Reserved
0x18	Reserved	

In order to maintain compatibility between booting configurations developed for the MPC5748G device that are migrated to the MPC5746C device, all references to CPU1 were marked as reserved. Bear in mind that there could be confusion as in the MPC5746C device only CPU0 (e200Z4) and CPU2 (e200z2) were implemented, CPU1 should not be configured.

4.2. Multi-Core

The multi-core strategy between the MPC5748G and MPC5746C device is the same in terms that the larger e200Z4 core is aimed to be the full-power application core, while the smaller e200Z2 core is aimed at low-power operation. Both cores can execute in RUN modes but only the e200Z2 core can execute in low-power consumption modes.

Unlike the MPC5748G device where all its derivatives have at least two cores (one e200Z4 and one e200Z2 in the smaller cases), the MPC5746C device has derivatives that are “single core”. These devices are virtually “single core” derivatives, as they actually have the same two cores, one e200Z4 for running modes and one e200z2 core for low-power modes. The difference with the dual core devices is that the two cores cannot run simultaneously.

4.3. Memory

Both the Flash and RAM memories are smaller on the MPC5746C device. The same Flash memory blocks size and architecture was maintained between the two devices, only some memory blocks were eliminated altogether to reduce the total memory size of smaller derivatives.

Table 5. Flash memory blocks on each device

Start Address	End Address	Block Name	In MPC5748G	In MPC5746C
Low Space Blocks				
0x00F8C000	0x00F8FFFF	16 KB code block - Low Block 0	Yes	Yes
0x00404000	0x00407FFF	BAF - read only - - Low Block 1	Yes	Yes
0x00FC0000	0x00FC7FFF	32 KB code block - Low Block 2	Yes	Yes
0x00FC8000	0x00FCFFFF	32 KB code block - Low Block 3	Yes	Yes
0x00FD0000	0x00FD7FFF	32 KB code block - Low Block 4	Yes	Yes
0x00FD8000	0x00FDFFFF	32 KB code block - Low Block 5	Yes	Yes
0x00FE0000	0x00FEFFFF	64 KB code block - Low Block 6	Yes	Yes
0x00610000	0x0061FFFF	16 KB HSM code block 2 - Low Block 7	Yes	Yes
0x00FF0000	0x00FFFFFF	64 KB code block - Low Block 8	Yes	Yes
0x00620000	0x0062FFFF	16 KB HSM code block 3 - Low Block 9	Yes	Yes
Mid Space Blocks				
0x00F90000	0x00F93FFF	16 KB code block - Mid Block 0	Yes	Yes
0x00F94000	0x00F97FFF	16 KB code block - Mid Block 1	Yes	Yes
0x00F98000	0x00F9BFFF	16 KB code block - Mid Block 2	Yes	Yes
0x00F9C000	0x00F9FFFF	16 KB code block - Mid Block 3	Yes	Yes
0x00FA0000	0x00FA3FFF	16 KB code block - Mid Block 4	Yes	Yes
0x00FA4000	0x00FA7FFF	16 KB code block - Mid Block 5	Yes	Yes
0x00FA8000	0x00FABFFF	16 KB code block - Mid Block 6	Yes	Yes
0x00FAC000	0x00FAFFFF	16 KB code block - Mid Block 7	Yes	Yes
0x00FB0000	0x00FB7FFF	32 KB code block - Mid Block 8	Yes	No
0x00FB8000	0x00FBFFFF	32 KB code block - Mid Block 9	Yes	No
High Space Blocks				
0x00F80000	0x00F83FFF	HSM data block 0 - High Block 0	Yes	Yes
0x00F84000	0x00F87FFF	HSM data block 1 - High Block 1	Yes	Yes
256K Blocks				
0x01000000	0x0103FFFF	256 KB Flash block 0	Yes	Yes
0x01040000	0x0107FFFF	256 KB Flash block 1	Yes	Yes
0x01080000	0x010BFFFF	256 KB Flash block 2	Yes	Yes
0x010C0000	0x010FFFFFFF	256 KB Flash block 3	Yes	Yes
0x01100000	0x0113FFFF	256 KB Flash block 4	Yes	Yes
0x01140000	0x0117FFFF	256 KB Flash block 5	Yes	Yes
0x01180000	0x011BFFFF	256 KB Flash block 6	Yes	Yes
0x011C0000	0x011FFFFFFF	256 KB Flash block 7	Yes	Yes
0x01200000	0x0123FFFF	256 KB Flash block 8	Yes	Yes
0x01240000	0x0127FFFF	256 KB Flash block 9	Yes	Yes
0x01280000	0x012BFFFF	256 KB Flash block 10	Yes	No
0x012C0000	0x012FFFFFFF	256 KB Flash block 11	Yes	No

Peripheral differences

<i>Start Address</i>	<i>End Address</i>	<i>Block Name</i>	<i>In MPC5748G</i>	<i>In MPC5746C</i>
0x01300000	0x0133FFFF	256 KB Flash block 12	Yes	No
0x01340000	0x0137FFFF	256 KB Flash block 13	Yes	No
0x01380000	0x013BFFFF	256 KB Flash block 14	Yes	No
0x013C0000	0x013FFFFF	256 KB Flash block 15	Yes	No
0x01400000	0x0143FFFF	256 KB Flash block 16	Yes	No
0x01440000	0x0147FFFF	256 KB Flash block 17	Yes	No
0x01480000	0x014BFFFF	256 KB Flash block 18	Yes	No
0x014C0000	0x014FFFFF	256 KB Flash block 19	Yes	No
0x01500000	0x0153FFFF	256 KB Flash block 20	Yes	No
0x01540000	0x0157FFFF	256 KB Flash block 21	Yes	No

On the other hand, the RAM block sizes were changed between the two devices. The next table describes the RAM memory block sizes on each device.

Table 6. **RAM memory blocks on each device**

<i>Start Address</i>	<i>End Address</i>	<i>MPC5746C Blocks</i>	<i>MPC5748G Blocks</i>
0x40000000	0x40001FFF	8 KB	8 KB
0x40002000	0x4000FFFF	56 KB	56 KB
0x40010000	0x4001FFFF	64 KB	64 KB
0x40020000	0x4002FFFF	64 KB	128 KB
0x40030000	0x4003FFFF	64 KB	
0x40040000	0x4004FFFF	64 KB	256 KB
0x40050000	0x4005FFFF	64 KB	
0x40060000	0x4007FFFF	-	
0x40080000	0x400BFFFF	-	256 KB

5. Peripheral differences

This section will describe the specific differences found on the MPC5748G and MPC5746C peripheral set. Even though the two devices share the same peripherals, there are some implementation differences that must be considered when migrating software from one device to another.

5.1. Crossbar (XBAR)

The Crossbar (XBAR) or Crossbar Switch (AXBS) architecture is one of the few peripherals that were drastically changed between the MPC5748G and MPC5746C devices. This is because the amount of masters on each device is also very different. The MPC5748G device required two XBARs in series to be able to accommodate the large amount of masters and slaves communication options. The MPC5746C has fewer masters and only one XBAR is required to interface them with the slaves.

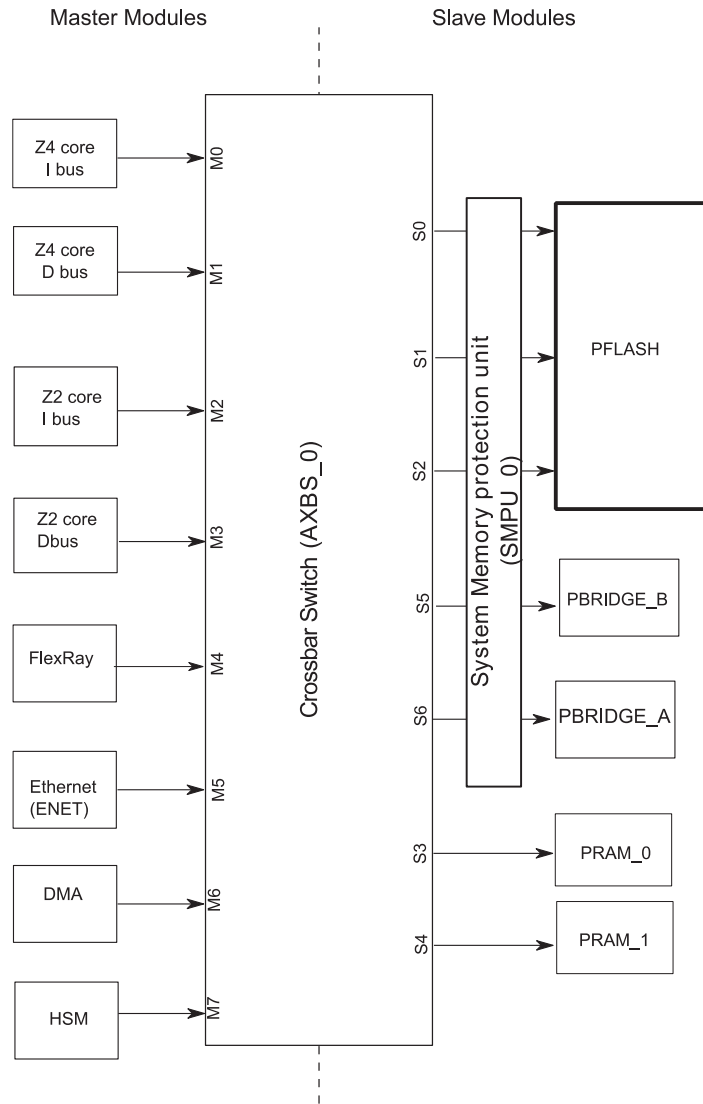


Figure 1. MPC5746C XBAR architecture

Peripheral differences

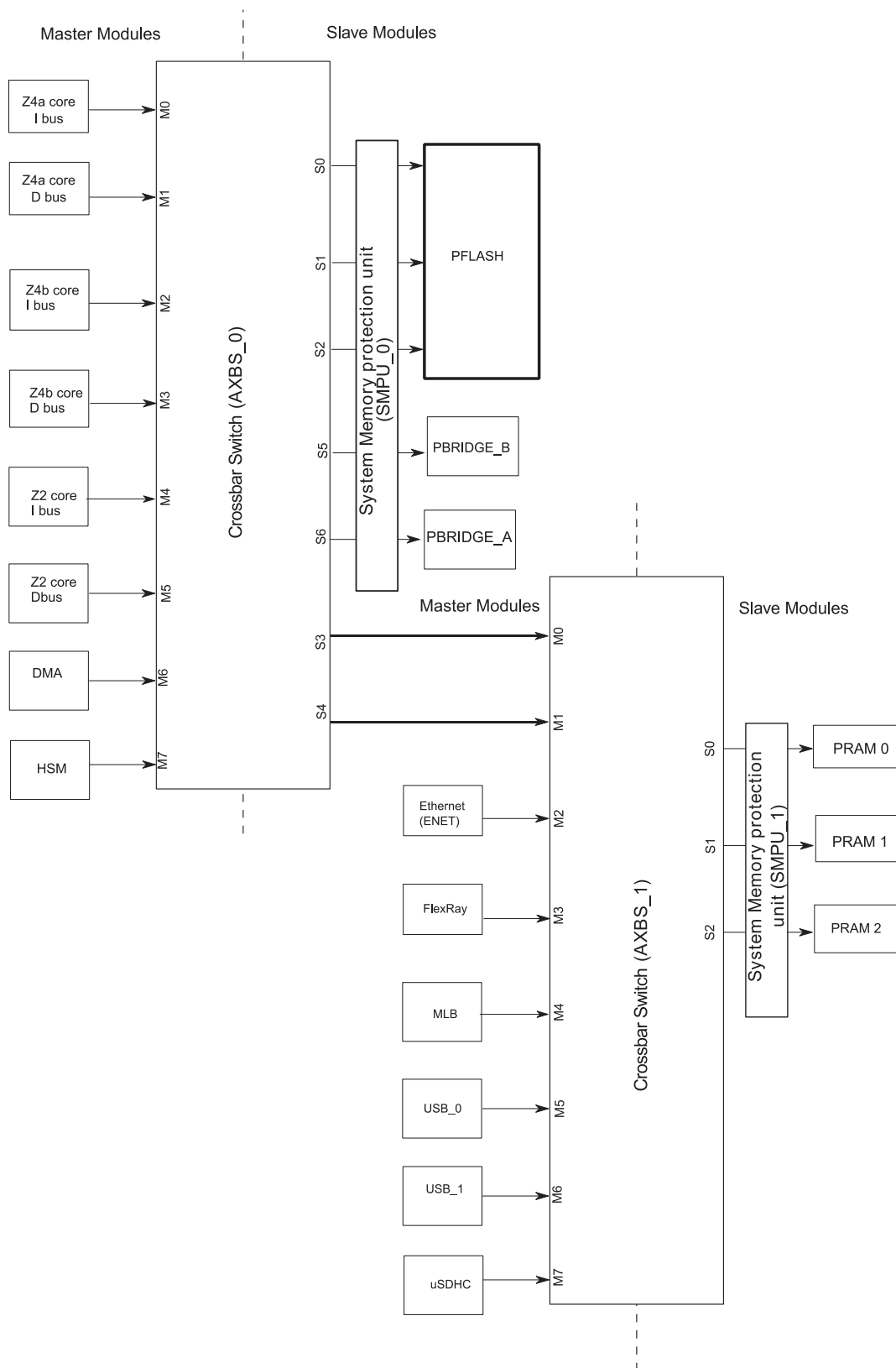


Figure 2. MPC5748G XBAR architecture

Figure 1 and Figure 2 describe the different XBAR architectures on each device. As can be noted, the master and slave ports are different for each device. These ports must be considered when migrating optimization configurations from one device to another.

In terms of performance, the MPC5746C performs slightly better on the Z4 to SRAM path when compared to the MPC5748G even when operating at 160 MHz. This is because the second XBAR is no longer present. While the XBAR architecture is very different between the two devices, the impact on functionality is minimal and only performance is slightly different.

5.2. Interrupt controller (INTC)

Since the MPC5746C device has two processors and the MPC5748G has three, the INTC module has changed to accommodate this difference. The register functionalities are also different so the user must be aware that the same register affects different cores on each device.

Table 7. INTC register differences between devices

<i>Register</i>	<i>MPC5748G affected core</i>	<i>MPC5746C affected core</i>
INTC_CPR0	Z4A	Z4
INTC_CPR1	Z4B	Z2
INTC_CPR2	Z2	not implemented
INTC_IACKR0	Z4A	Z4
INTC_IACKR1	Z4B	Z2
INTC_IACKR2	Z2	not implemented
INTC_EOIR0	Z4A	Z4
INTC_EOIR1	Z4B	Z2
INTC_EOIR2	Z2	not implemented

The INTC driver must be adapted so that the actual core that wants to be configured is being affected by the application code accessing the CPRn, IACKRn or EOIRn registers.

Unlike the just mentioned registers whose core numbering scheme was changed. This is not always the case. The INTC_PSRn register allows the application code to indicate which core must process an interrupt request. The PRC_SELN bit allows to select this core for each interrupt source (refer to Figure 3). For the PRC_SELN register, the core numbering is the same for both devices:

- Processor 0 is Z4A for MPC5748G or the only Z4 on MPC5746C
- Processor 1 is Z4B for MPC5748G and is not implemented on MPC5746C
- Processor 2 is Z2 for both devices
- Processor 3 is the Hardware Security Module (HSM) for both devices

Peripheral differences

Bit	0	1	2	3	4	5	6	7
Read	PRC_SELN				0			SWTN
Write								
Reset	1	0	0	0	0	0	0	0
Bit	8	9	10	11	12	13	14	15
Read	0				PRIN			
Write								
Reset	0	0	0	0	0	0	0	0

n

Field	Description																																
0–3 PRC_SELN	<p>Processor select bits. If an interrupt source is enabled, PRC_SELn[3:0] selects whether the interrupt request is to be sent to processor 0, processor 1, processor 2, processor 3, or any combination.</p> <table border="0"> <tr><td>0000</td><td>No interrupt request sent</td></tr> <tr><td>0001</td><td>Interrupt request sent to processors 3</td></tr> <tr><td>0010</td><td>Interrupt request sent to processors 2</td></tr> <tr><td>0011</td><td>Interrupt request sent to processors 2, 3</td></tr> <tr><td>0100</td><td>Interrupt request sent to processors 1</td></tr> <tr><td>0101</td><td>Interrupt request sent to processors 1, 3</td></tr> <tr><td>0110</td><td>Interrupt request sent to processors 1, 2</td></tr> <tr><td>0111</td><td>Interrupt request sent to processors 1, 2, 3</td></tr> <tr><td>1000</td><td>Interrupt request sent to processors 0</td></tr> <tr><td>1001</td><td>Interrupt request sent to processors 0, 3</td></tr> <tr><td>1010</td><td>Interrupt request sent to processors 0, 2</td></tr> <tr><td>1011</td><td>Interrupt request sent to processors 0, 2, 3</td></tr> <tr><td>1100</td><td>Interrupt request sent to processors 0, 1</td></tr> <tr><td>1101</td><td>Interrupt request sent to processors 0, 1, 3</td></tr> <tr><td>1110</td><td>Interrupt request sent to processors 0, 1, 2</td></tr> <tr><td>1111</td><td>Interrupt request sent to processors 0, 1, 2, 3</td></tr> </table>	0000	No interrupt request sent	0001	Interrupt request sent to processors 3	0010	Interrupt request sent to processors 2	0011	Interrupt request sent to processors 2, 3	0100	Interrupt request sent to processors 1	0101	Interrupt request sent to processors 1, 3	0110	Interrupt request sent to processors 1, 2	0111	Interrupt request sent to processors 1, 2, 3	1000	Interrupt request sent to processors 0	1001	Interrupt request sent to processors 0, 3	1010	Interrupt request sent to processors 0, 2	1011	Interrupt request sent to processors 0, 2, 3	1100	Interrupt request sent to processors 0, 1	1101	Interrupt request sent to processors 0, 1, 3	1110	Interrupt request sent to processors 0, 1, 2	1111	Interrupt request sent to processors 0, 1, 2, 3
0000	No interrupt request sent																																
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1011	Interrupt request sent to processors 0, 2, 3																																
1100	Interrupt request sent to processors 0, 1																																
1101	Interrupt request sent to processors 0, 1, 3																																
1110	Interrupt request sent to processors 0, 1, 2																																
1111	Interrupt request sent to processors 0, 1, 2, 3																																

Figure 3. INTC_PSRn register bit options

The user must be careful as the core numbers are not the same on all the contexts.

5.3. Ethernet (ENET)

The ENET architecture implementation for both devices is different in the way that the MPC5748G has more connectivity options than the MPC5746C. The former device has two independent ENET modules, while the latter only has one. The implementation on both is exactly same, so both devices offer Audio Video Bridging (AVB) enhancements such as transmission and reception multi-queue, RX parser features, and traffic shaping algorithms.

Other considerable difference on the Ethernet interface of the devices is that the MPC5748G device has a Layer 2 Ethernet Switch which connects the two independent ENET modules to create a network. The MPC5746C device does not have an embedded switch so it can only participate on an Ethernet network as an end node.

In terms of functionality, the MPC5746C includes a fix for errata e7885 that the MPC5748G does not have. If a driver is being ported from the MPC5748C to the MPC5748G, then the workaround described on the MPC5748G errata document must be included on the driver.

5.4. Input Glitch Filter (IGF)

The MPC5746C device introduces the Input Glitch Filter module that provides programmable glitch rejection on some digital inputs. This IGF is placed between the SIUL2 module and the various peripherals on the MCU.

When migrating a driver from the MPC5748G to the MPC5746C device, it could be useful to include glitch filter configurations to ensure that the input signals are as clean as possible.

6. Conclusion

Both the MPC5748G and the MPC5746C devices share almost every peripheral and migration between them is mostly straightforward. This application note describe the aspects where the user must be especially careful when considering scaling from one device member to the next. Please refer to the devices Reference Manuals and Datasheets for the most updated information at freescale.com.



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