Freescale Semiconductor, Inc.
Application Note

Document Number: AN5148
Rev. 0, 06/2015

Avoiding MPC574x Multiple Resets During Slow Power Ramp

By: Alasdair Robertson

Contents

1. Introduction

The MPC5748G MCU is a multi-core, high performance Power Architecture® based microcontroller targeted for automotive gateway and body applications. It is also equally suited to other applications because of rich communication peripheral set and embedded Hardware Security Module (HSM).

During power on, if the main supply voltage is ramped very slowly, multiple resets may be observed during the phase when the voltage is still ramping. These resets are totally expected behavior and do not have any negative impact on the microcontroller operation. This document explains:

- Why these resets occur
- When you would expect to see them
- How to reduce the likelihood of resets during power ramping in an application

2. Observing the resets

Before explaining why multiple resets occur during power on, it is useful to show some scope plots of the observed behavior and explain the conditions that make multiple resets more likely.

2.1. Test Configuration

- The MPC5748G is being run on the Freescale MPC574xx evaluation board.
- The device is configured to run from 3.3 V on VDD_HV_x domains and using the internal regulator with external ballast transistor (also powered from the same 3.3 V supply). The flash is also powered from 3.3 V supply.
- Very simple application code is programmed into the MCU flash which executes from reset and configures the system clock to 160 MHz. The code then enters a continuous loop toggling an LED, allowing code execution to be observed.
- An external programmable power supply is used to power the MCU 3.3 V domain.

With a ramp rate in the region of 0.1 V per second on the main supply line, the following plot is seen on the scope.

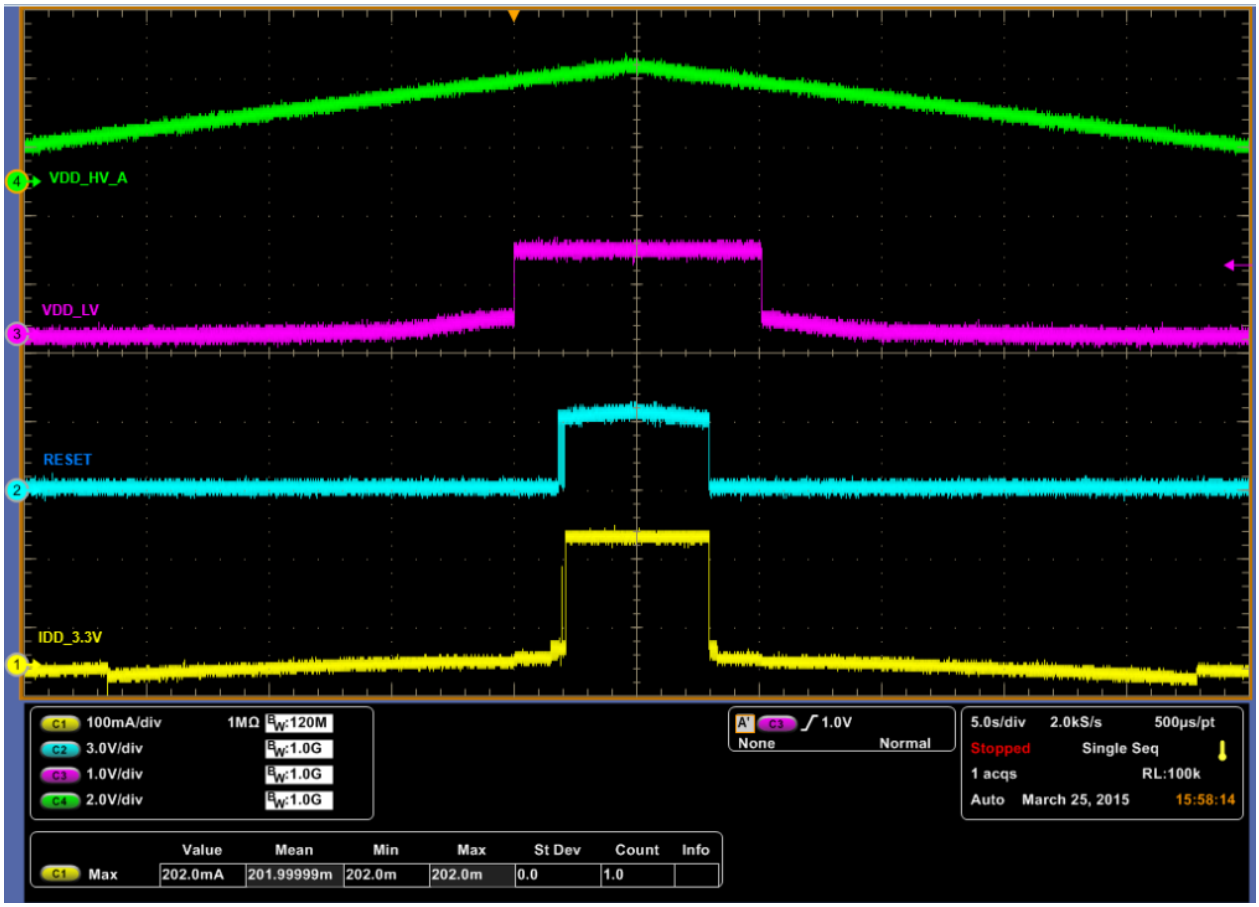

Figure 1. VDD_3.3 V ramp rate of 0.1 V per second

Key:

- The green trace shows the Input voltage from the programmable power supply (the 3.3 V supply line to the MCU and external ballast transistor)
- The purple trace shows the VDD_LV input to the MCU, supplied from the external ballast transistor (this is here simply as a reference point)
- The blue trace shows the MCU_RESET signal from the MCU
- The yellow trace shows the current (via a current probe) of the 3.3 V supply line from the programmable power supply. Since this is supplying both the MCU and the EVB 3.3 V peripherals, this is a little higher than the operating current of the MCU which is not important as we are looking at the current trend in these plots.

Looking at the leading (rising) edge of the RESET "pulse", it can just be seen that there are multiple transitions happening at this point. There are also noticeable multiple transitions on the IDD_3.3V plot at the same point. Zooming into this area shows the following plot. Here we can see that the RESET line is driven low 40 times, approximately 7.5 ms apart as the VDD_HV_A very slowly rises (not visible in this timebase setting)

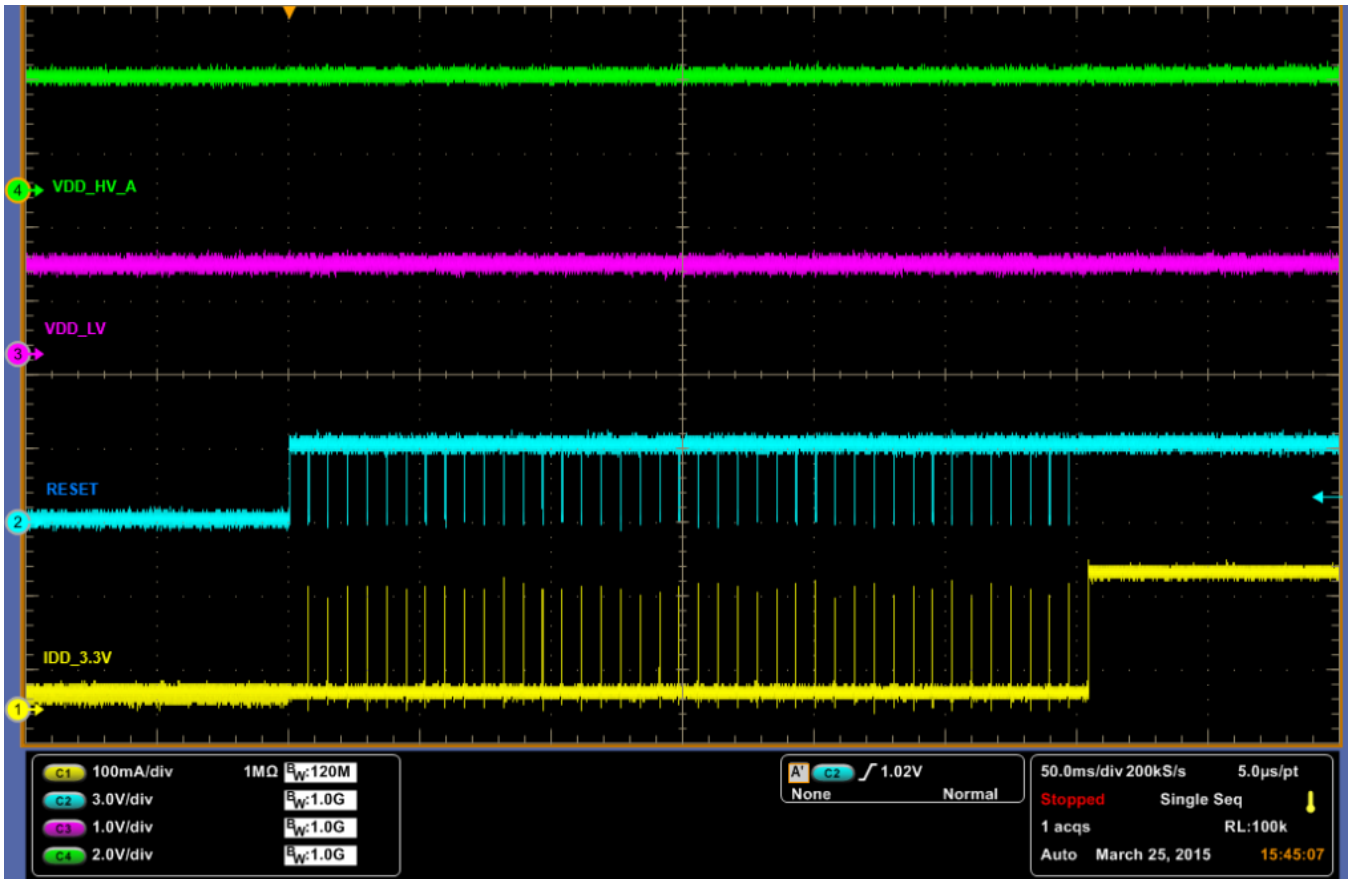

Figure 2. VDD_3.3 V ramp rate of 0.1 V per second – Zoomed in

3. LVD and Cause of the Resets

So what is causing these resets and what is the impact of this in a real application?

Before answering this question, it is important to understand some of the internal MCU circuitry which is designed to ensure safe and reliable operation of the device at all times. There are various Low Voltage Detection (LVD) circuits that continuously monitor the voltage levels on the following voltage domains:

- **VDD_HV_A:** Main supply for all internal regulators (including core and flash) as well as peripheral domain A.
- **VDD_HV_FLA:** 3.3 V flash power supply (either regulated internally when VDD_HV_A = 5 V or supplied externally if VDD_HV_A = 3.3 V).
- **VDD_LV:** 1.25 V Core voltage supply which can be supplied from an internal regulator for low current applications, internal regulator with external ballast or from an external supply.

Should the voltage on one of these domains drop below a critical level, the LVD triggers a RESET to ensure that nothing non deterministic happens (such as the memories starting to read incorrect data or the core starting to fail).

During power on, the MCU is held in reset until all of the voltages have risen above the LVD threshold at which point the device is guaranteed to operate normally. Only after this point is reset released and the normal device boot sequence starts with the SSCM reading the DCF clients from the UTEST and then the core executing code from the BAF.

So, if we now consider the situation where we are seeing multiple resets with a slow power ramp, this is easily explained:

- As the VDD_3.3 voltage is slowly increased, the LVD's hold the device in reset until all of the LVD's have been released. At this point, the supply voltage is just marginally above the last LVD to release (which will be either the VDD_FLASH or VDD_HV_A LVD). It is also important to note that although the LVD's have released, the device will still be operating below the guaranteed operating range specified in the datasheet.
- The device now starts to boot, via the BAF to the application code. In this example, the application code quickly ramps the system clock to the maximum frequency of 160 MHz. This increase in current causes a drop in the 3.3 V supply. Since the supply is ramping very slowly, this voltage drop is sufficient to trip the LVD forcing the device to reset.
- This will continue to occur during ramp until the supply voltage is sufficient such that the drop in voltage when the device boots is above the LVD threshold.
- This is fully expected behavior and as such the device is functioning in a safe state to ensure operation is always reliable.
- The effect can also be observed by applying a steady state voltage at the point where reset has just been de-asserted (on this device on the bench this occurs at around 3.05 V) as shown in the screen capture below.

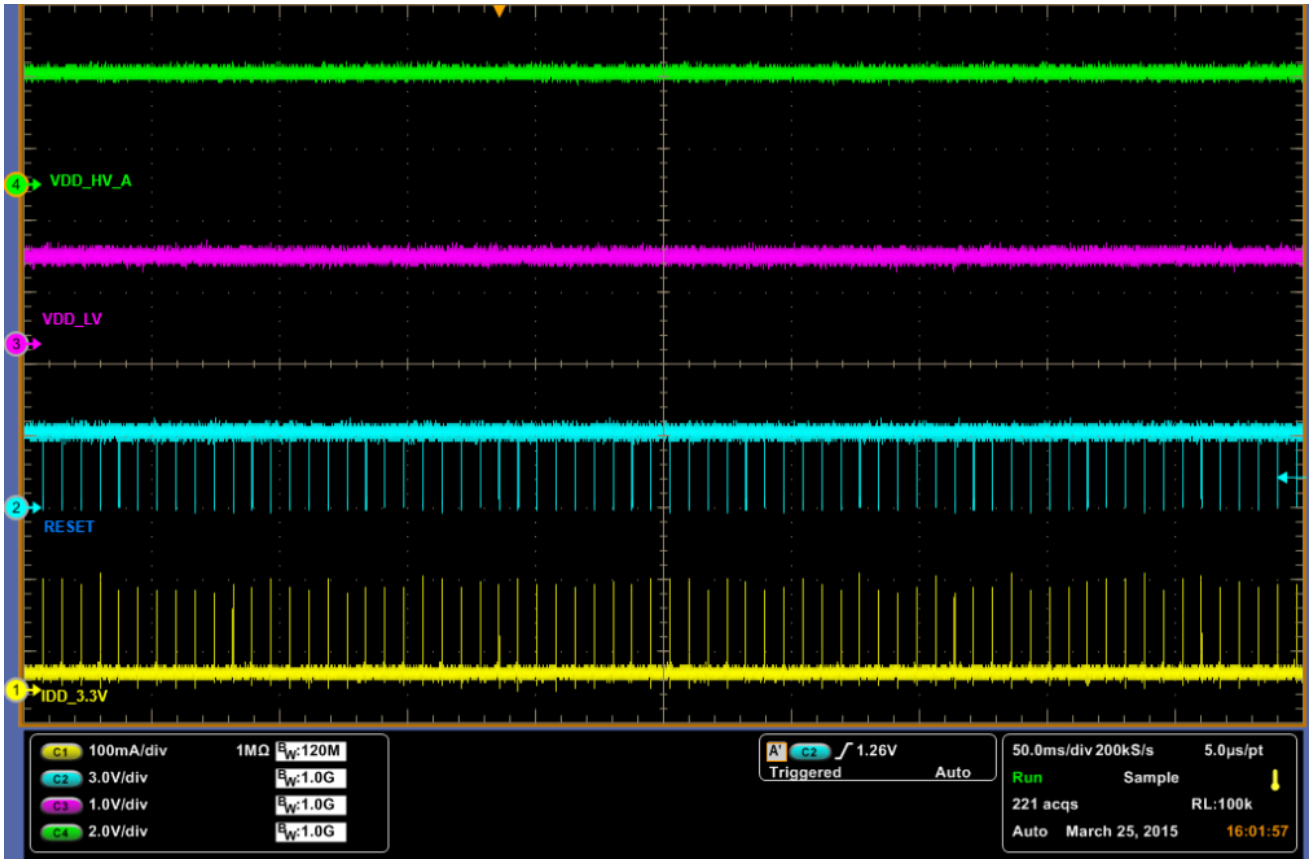

Figure 3. Steady state Reset toggle with VDD_3.3V at approximately 3.05 volts

4. Reducing the likelihood of Resets on power-up

As per the scope captures, it can be seen that the multiple resets only occur:

- During an extremely slow VDD ramp, in this case in the region of 0.1 V per second which is significantly slower than any real life situation.
- When VDD is held at the voltage just above the point that reset has been de-asserted (all the LVD's are released). To reiterate at this point, the supply voltage is still below the guaranteed operating range specified in the datasheet.

4.1. Initial configuration

From Power-on, the MCU is configured to exit reset with the 16 MHz Fast Internal Reference Clock (FIRC) routed to the system clock. In addition all of the peripherals are clock gated. This is a fairly low power state (10^{th} of mA) and is unlikely to cause issues during normal power ramping.

If on the other hand, the application code enables all of the peripherals and configures the system clock to the maximum using the PLL (all of which can be activated in a single mode change), the current increase is huge and the resultant voltage drop on the supply lines can trigger LVD reset(s).

To avoid multiple resets on power up there are various things that can be done as described in the following sections.

4.2. Power supply ramp rate

Ensure that the power supply ramp rate is not too slow and is within specification. In the bench tests to create this application note, the reset toggles start to occur when the main supply ramp rate is slower than 0.1 V per second, however this is highly dependent on setup and what your code is doing immediately after boot (clock settings, active cores etc.)

4.3. Peripheral Gating

Rather than enabling all of the peripherals in a single shot, peripherals can be enabled as required or in a staggered manner to reduce current spikes.

4.4. Progressive Clock Switching

Progressive Clock Switching (PCS) allows the system clock frequency to be slowly ramped to the desired target frequency rather than going from the 16 MHz IRC to the normal PLL clock in a single step (which causes a large current inrush).

The effect of progressive clock switching can be seen in the scope plots below. In both of these examples, the system clock frequency is configured as 160 MHz via the PLL driven from the external oscillator.

In the 1st plot, PCS is disabled. The current shown in the yellow trace ramps from 20 mA to approximately 200 mA in about 20 µs with an initial spike to 180 mA in 5 µs or so. This results in a large inrush current. The regulator cannot respond quickly enough to the increase in current and the voltage therefore drops. Local bulk storage capacitors can help to some degree with this but these are expensive and can cause problems in other areas.

Note that the PLL can also be manually ramped by the application software to achieve the same effect as PCS.

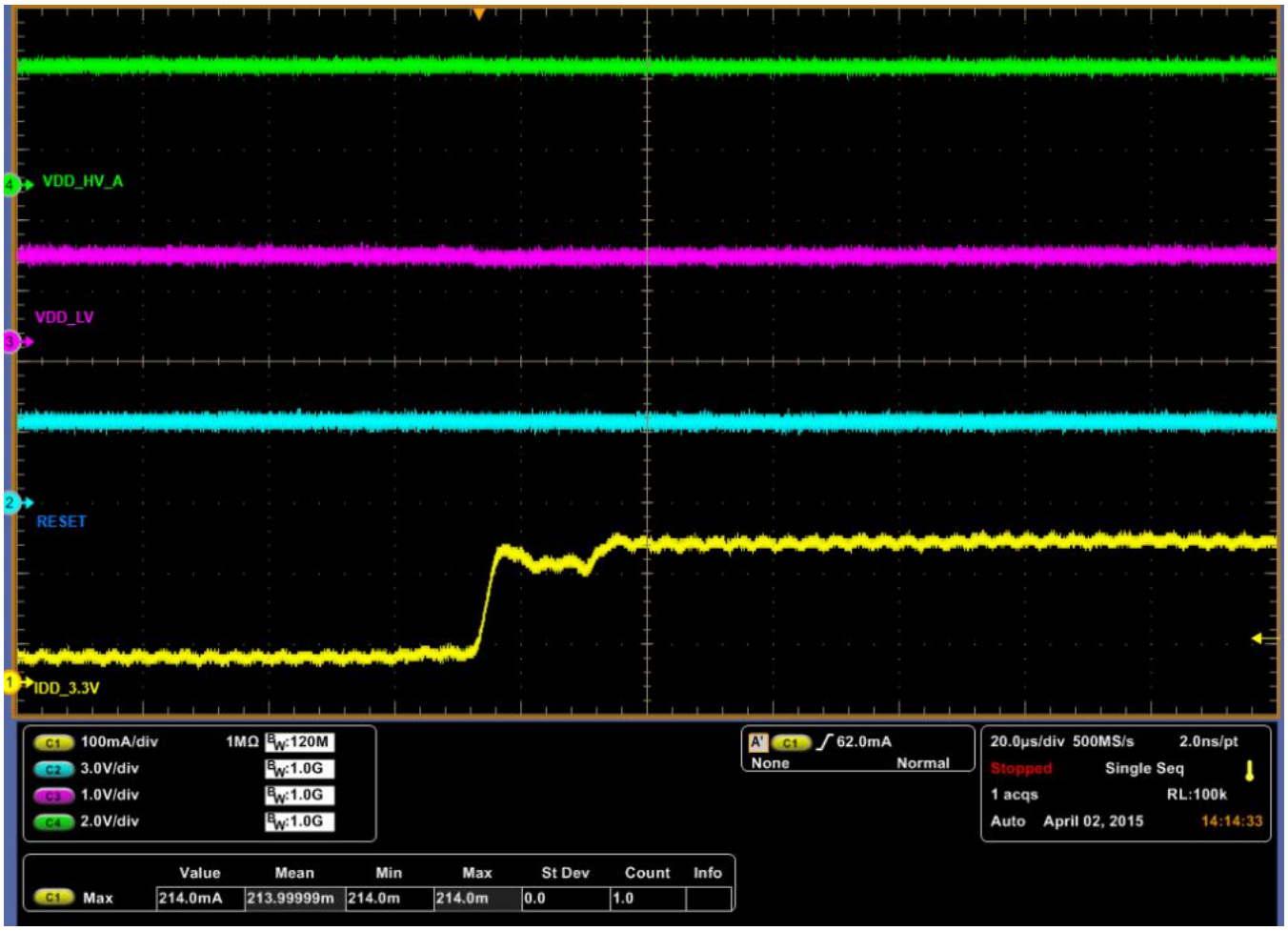

Figure 4. Current profile on VDD_3.3 with PCS disabled

With progressive clock switching enabled and configured for minimum ramp, the following plot shows the current profile again (yellow trace). In this instance the current is slowly increased with no real spikes taking something like 120 us to reach full operating current. This slower current ramp means the regulator has much longer to react to the increasing current and there is much less chance of a corresponding voltage drop.

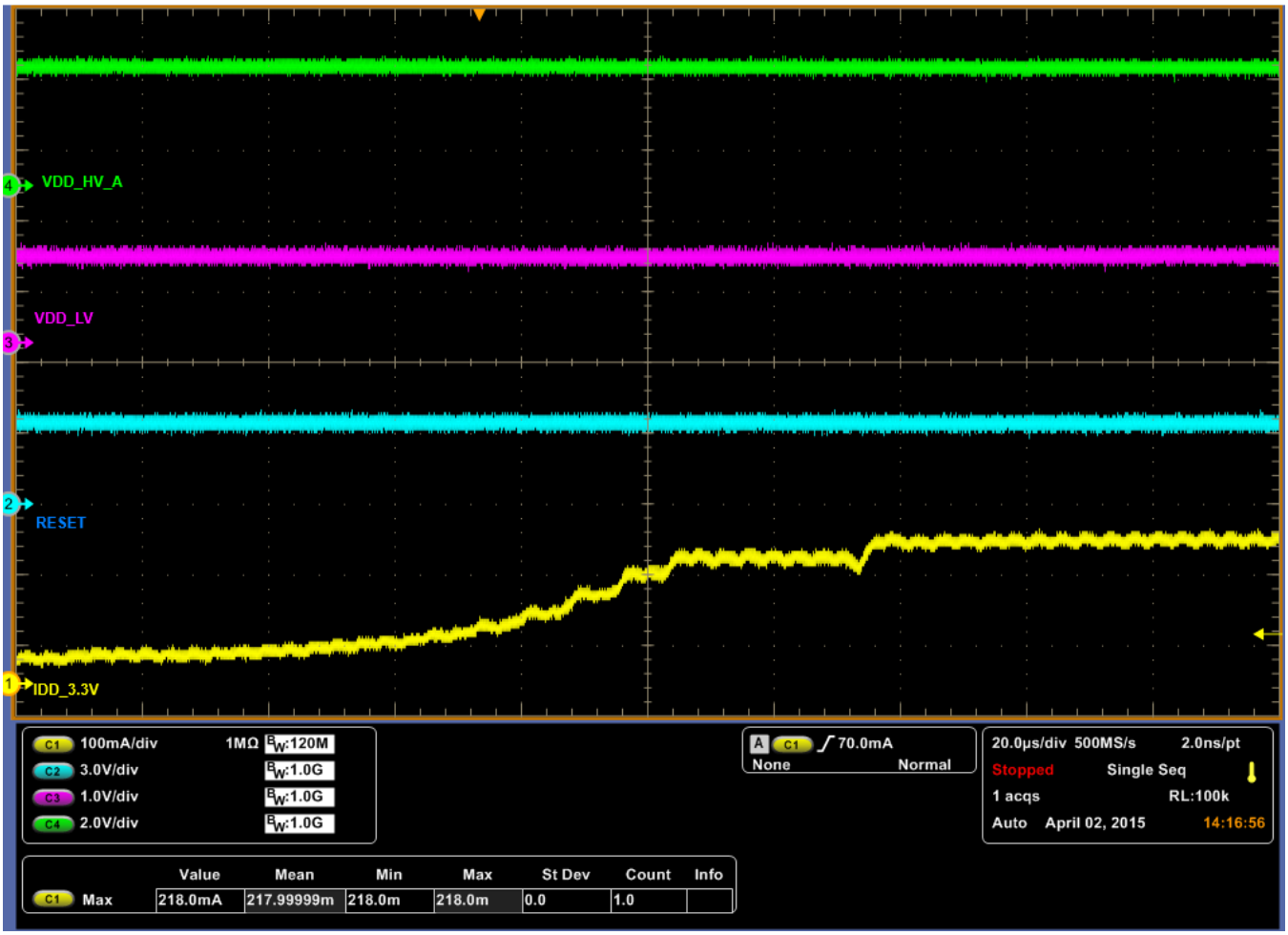

Figure 5. Current profile on VDD_3.3 with PCS enabled

To quantify the effect of PCS, the ramp rate test was re-run with PCS disabled and then enabled (all other settings are the same including ramp rate, application code, hardware setup). As can be seen in the plots below, with PCS disabled the reset toggling is very evident. In the 2nd plot with PCS enabled, the effect of reset toggling is no longer observed.

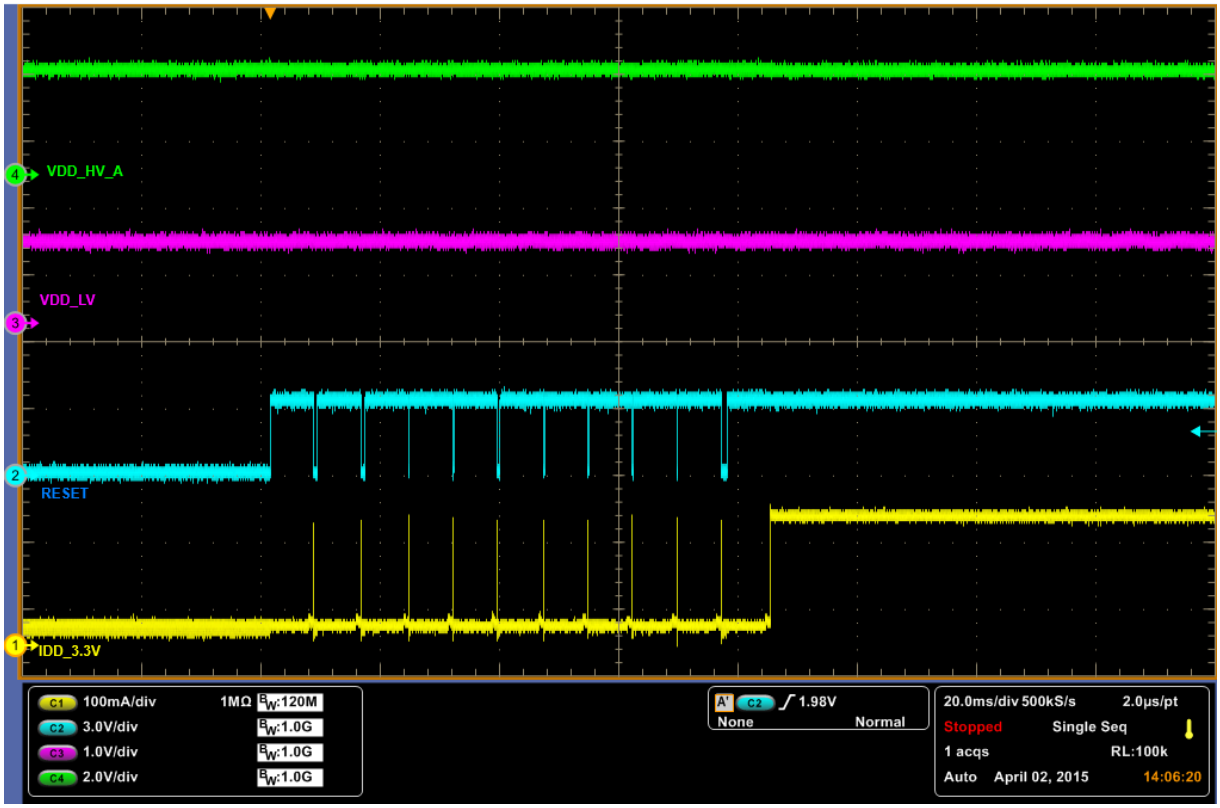

Figure 6. VDD_3.3V ramp rate of 0.1 V per second, Zoomed in – PCS Disabled

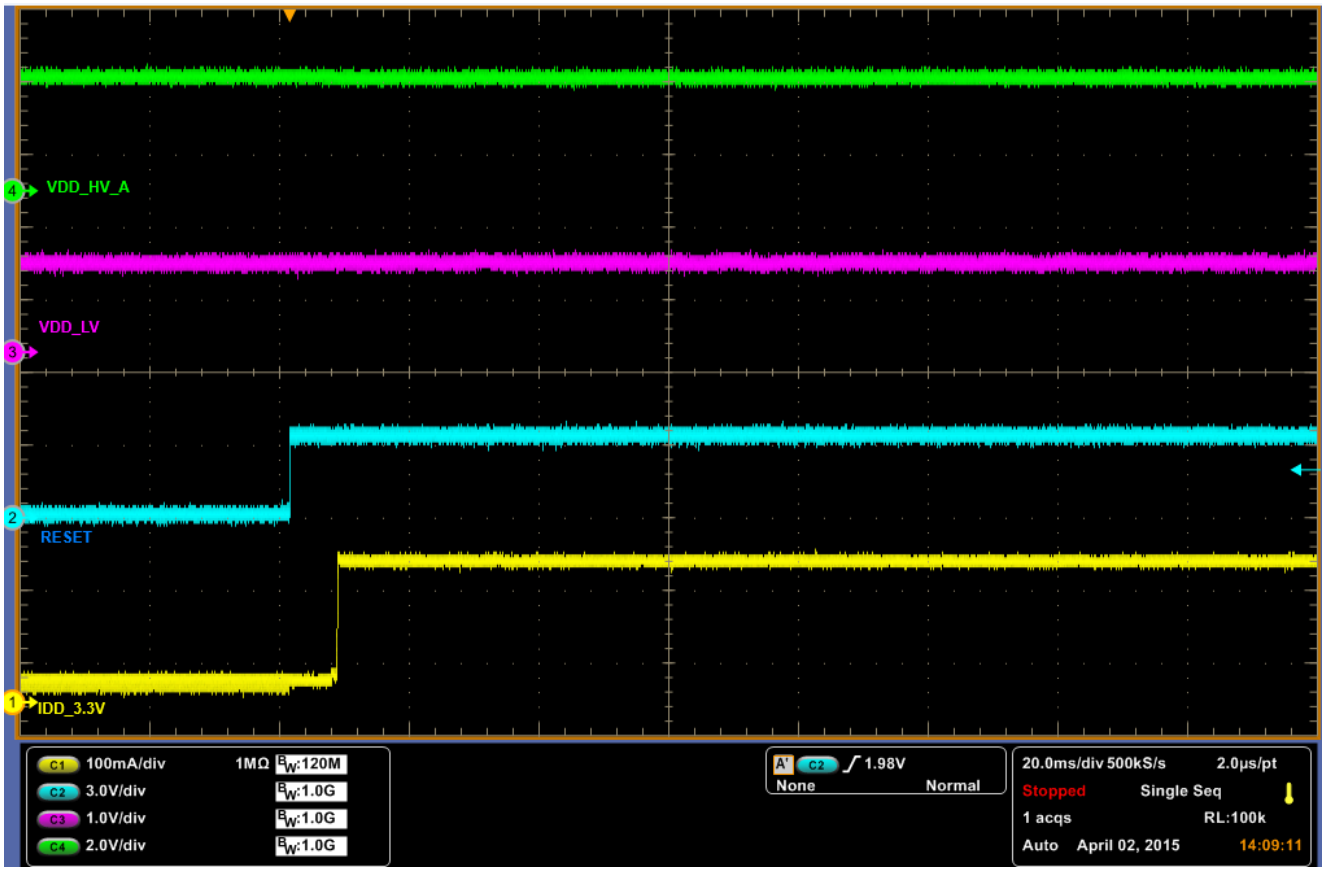

Figure 7. VDD_3.3V ramp rate of 0.1 V per second, Zoomed in – PCS Enabled

It is also observed that with PCS enabled, there is no “steady state” toggling of reset. The reset line toggles high when VDD_HV_A reaches 3.053 V with no toggling evidence.

5. Conclusion

With a slow ramp rate on the main power supply rail, it can be seen that the reset line may toggle multiple times as the voltage slowly increases, especially if the application code enables the PLL and sets the system clock to the maximum. This is expected behavior caused by a voltage drop when the system clock frequency is changed which in turn causes the Low Voltage monitoring circuit to trigger a reset (recall at this point, the supply voltage is still below the guaranteed operating range specified in the datasheet).

With a typical voltage supply ramp rate it is not expected that this effect will be observed. By enabling PCS, the impact on the power supply during frequency change is much reduced and further reduces the likelihood of seeing a reset toggle during power supply ramping.

How to Reach Us:

Home Page:
freescale.com

Web Support:
freescale.com/support

Document Number: AN5148
Rev. 0
06/2015