Freescale Semiconductor, Inc.
Engineering Bulletin

Document Number: EB832
Rev. 0, 02/2016

i.MX 6SoloX Application Processor Silicon Revision 1.2 to 1.3 Comparison

1. Introduction

This document provides information on the changes in the i.MX 6SoloX Application Processor between silicon revisions 1.2 and 1.3.

Contents

2. Changes Between Silicon Revisions 1.2 and 1.3

Table 1 lists the changes between i.MX 6Solo silicon revisions 1.2 and 1.3. Where an erratum is fixed, the relevant erratum number is provided with a high-level description.

Table 1. Changes between silicon revisions 1.2 and 1.3

Issue number	Description	Software impact of change	Silicon revision fix	Documented in silicon errata revision 1
-	Updated contents of chip silicon version register (USB_ANALOG_DIGPROG): • 0x00620001 for silicon revision 1.1 • 0x00620002 for silicon revision 1.2 • 0x00620003 for silicon revision 1.3	U-Boot reads the ROM revision contents to determine the silicon revision. The ROM revision number may not match the silicon revision number (e.g., ROM revision 1.5 means silicon revision 1.3).	Updated in 1.3	N/A
-	Updated value of the SI_REV[3:0] fuses: • “0” for silicon revision 1.1 • “1” for silicon revision 1.2 • “1” for silicon revision 1.3	Customer’s software using this value may need to be updated. Freescale BSPs do not read SI_REV[3:0].	Updated in 1.3	N/A
-	ROM ID	The ROM version number is not modified, because there are no ROM changes in silicon revision 1.3.	N/A	N/A
-	JTAG ID	The JTAG ID is not modified in silicon revision 1.3.	N/A	N/A
-	Product Markings	The part number does not change for silicon revision 1.3 and continues to end in suffix “AB”. The mask number indicated on the package for silicon revision 1.3 devices changes from “2N19K” to “3N19K”.	N/A	N/A
ERR009572	RDC: Access to RDC registers causes the CPU to hang if the PCIE_DISABLE fuse disables PCIe	i.MX 6SoloX Silicon Revision 1.2 devices without the PCIe_DISABLE fuse programmed (date code 1524 or later) and Silicon Revision 1.3 devices with the design fix do not have any software impact, because the latest Freescale Linux® BSP releases clock gates the PCIe modules clocks by default. Customers using other operating systems need to ensure the clock of the PCIe module is gated off for maximum power savings, because fuses are no longer programmed to disable the PCIe module clocks. The CCM_CCGR4 [1:0] register in the CCM module should be programmed to clock gate the PCIe module’s clock root by the application software.	Fixed in 1.3	Yes
ERR009636	MMDC: Random data corruption during reads from DDR memory	No software impact.	Fixed in 1.3	Yes

3. Software/ROM Changes from Silicon Revision 1.2 to 1.3

No i.MX 6SoloX ROM code changes are made between silicon revisions 1.2 and 1.3.

4. Revision History

Table 2. Revision history

Revision number	Date	Substantive change
0	02/2016	Initial release

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